

David W. Sney

IMAGE WEST COMPUTER  
ANIMATION PROJECT

845 N. HIGHLAND AVE.  
HOLLYWOOD, CA 90038  
(213)-466-4181



mead

NF 3980

\$ .79

TX

01746



notebook

11 In. x 8½ In.

40 Sheets

Wide Marginal Ruled

06-3520

THE MEAD CORPORATION, DAYTON, OHIO 45463



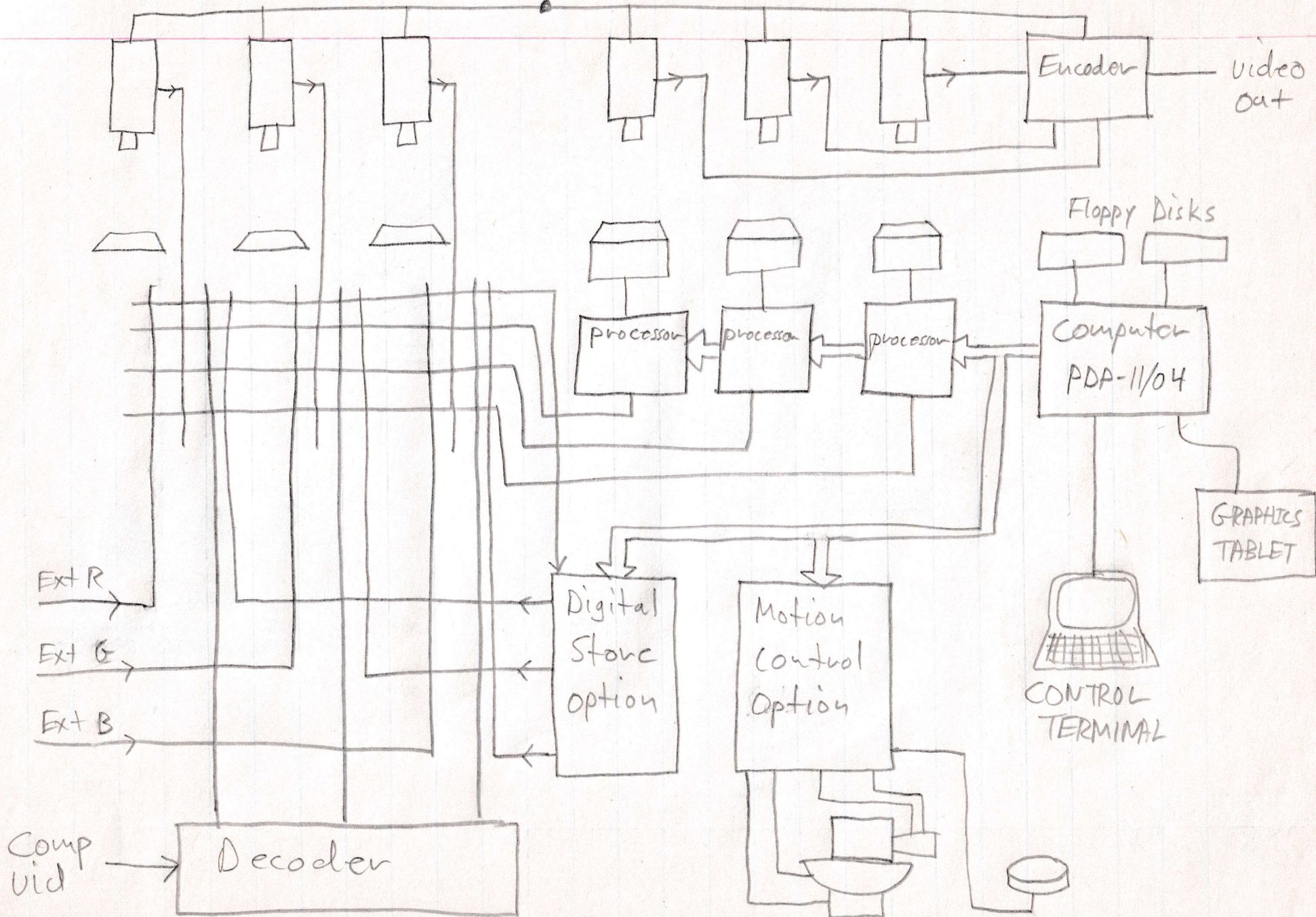


Switchable Stds  
Sync gen

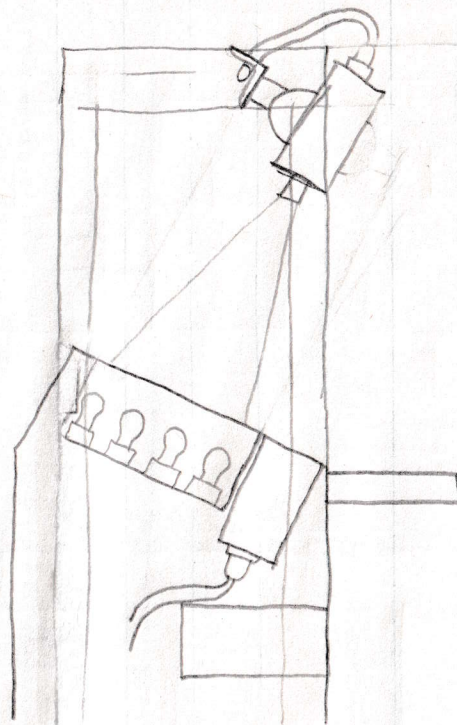
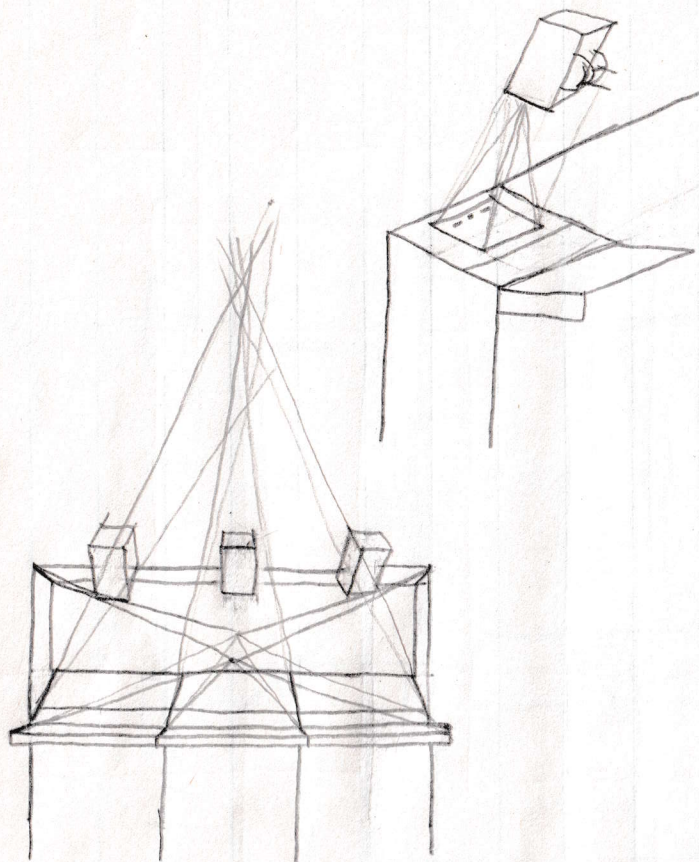
Min Dev  
Ler Info

11/10

11/30





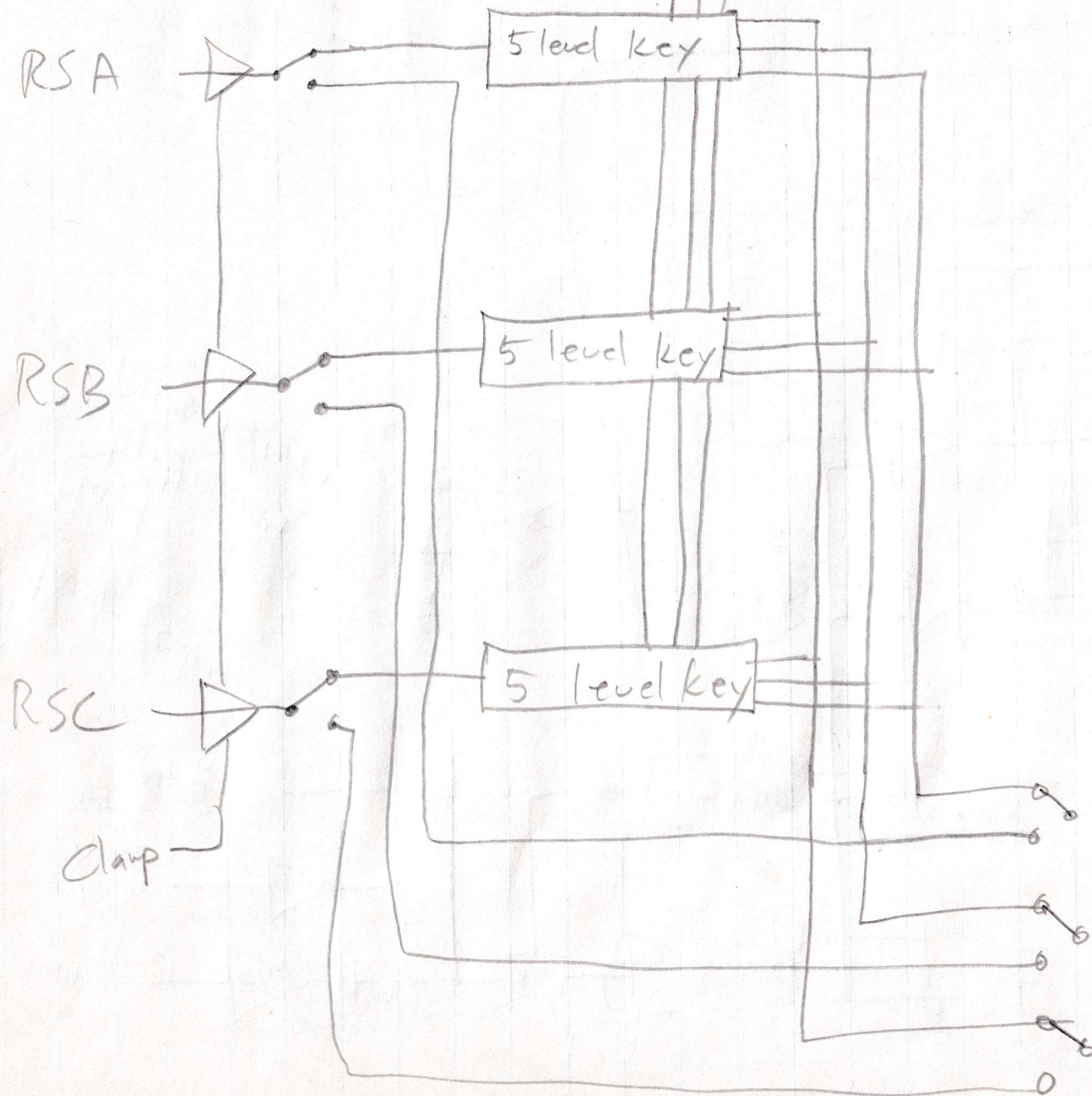


$$\begin{array}{r} 0.75 \\ 8 \overline{) 6} \\ \underline{56} \\ 40 \end{array}$$

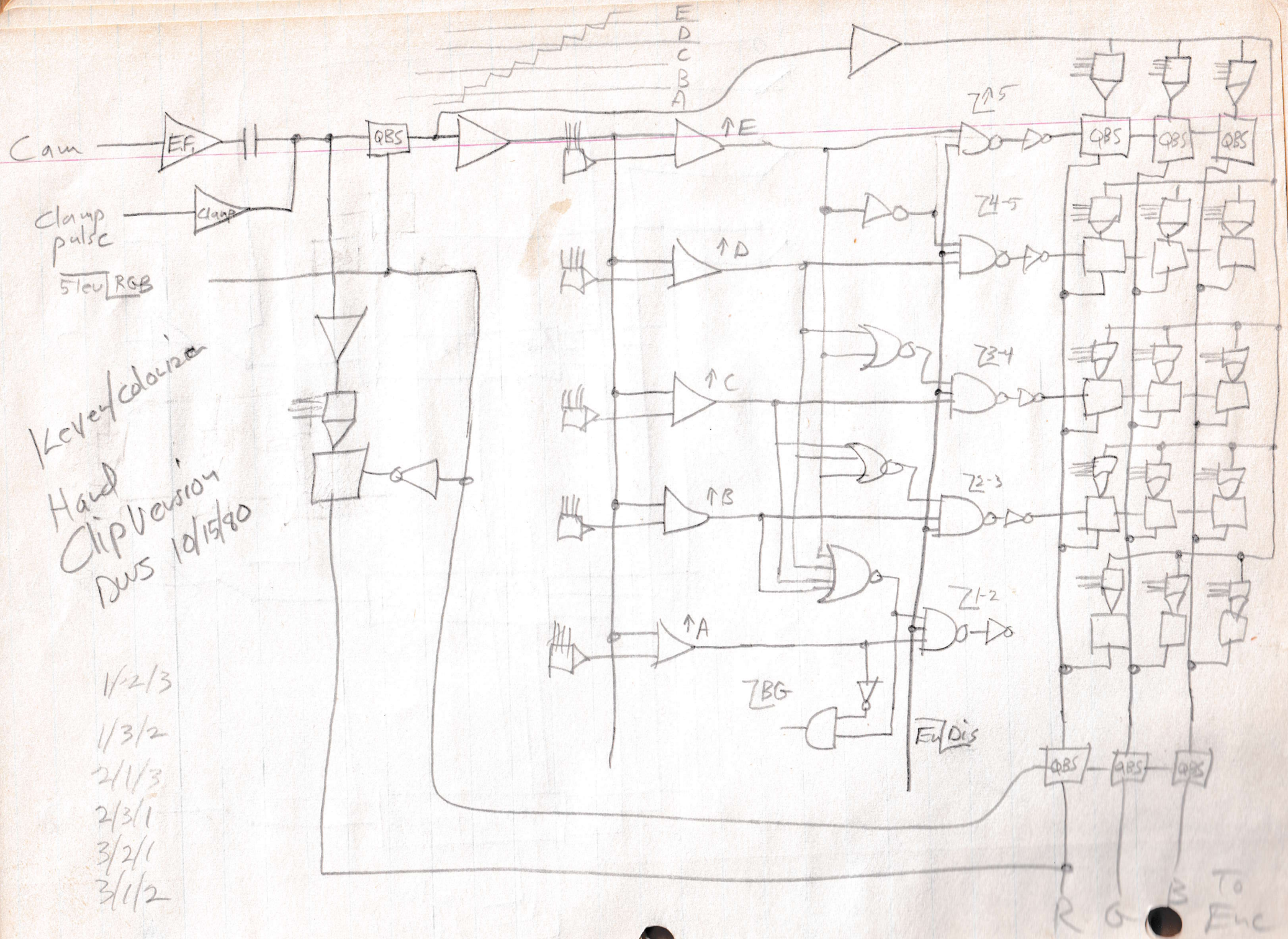
*Handwritten signature or scribble.*



Priority  
Logic







Level/colorizer  
Hand  
Clip Version  
DWS 10/15/80

- 1/2/3
- 1/3/2
- 2/1/3
- 2/3/1
- 3/2/1
- 3/1/2

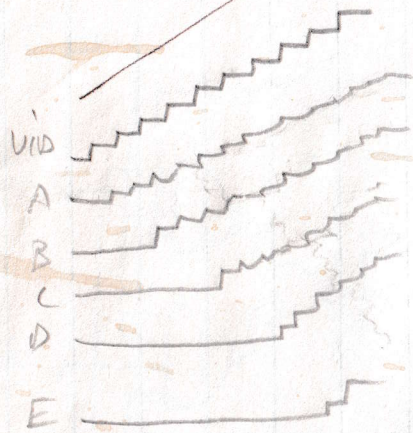
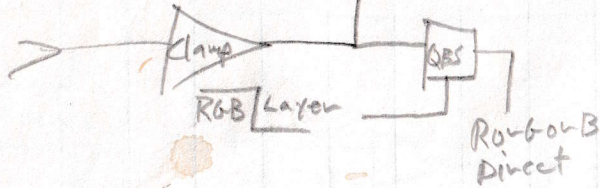


linear clip  
Kcton/colorizer  
PWS 10/15/80

digitally controlled  
gain (gray level band width)

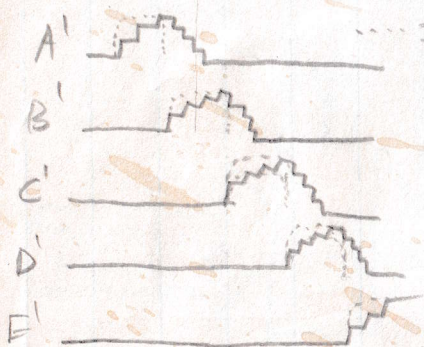
Digital Color Regs

Roscam  
Cam

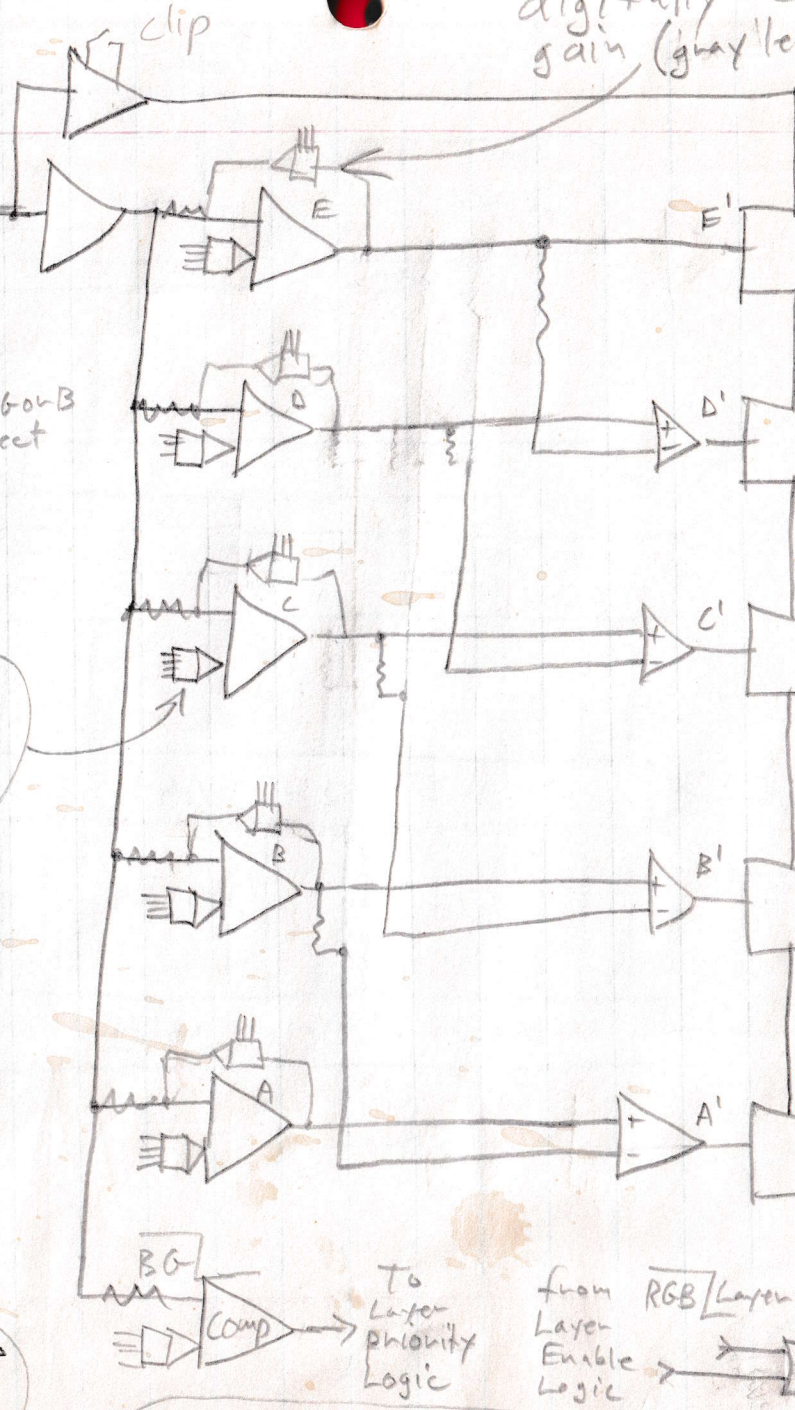


clip level  
set by  
D/A C's

Effects of  
Max gain



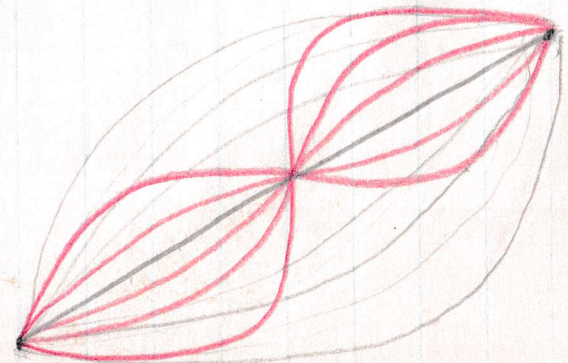
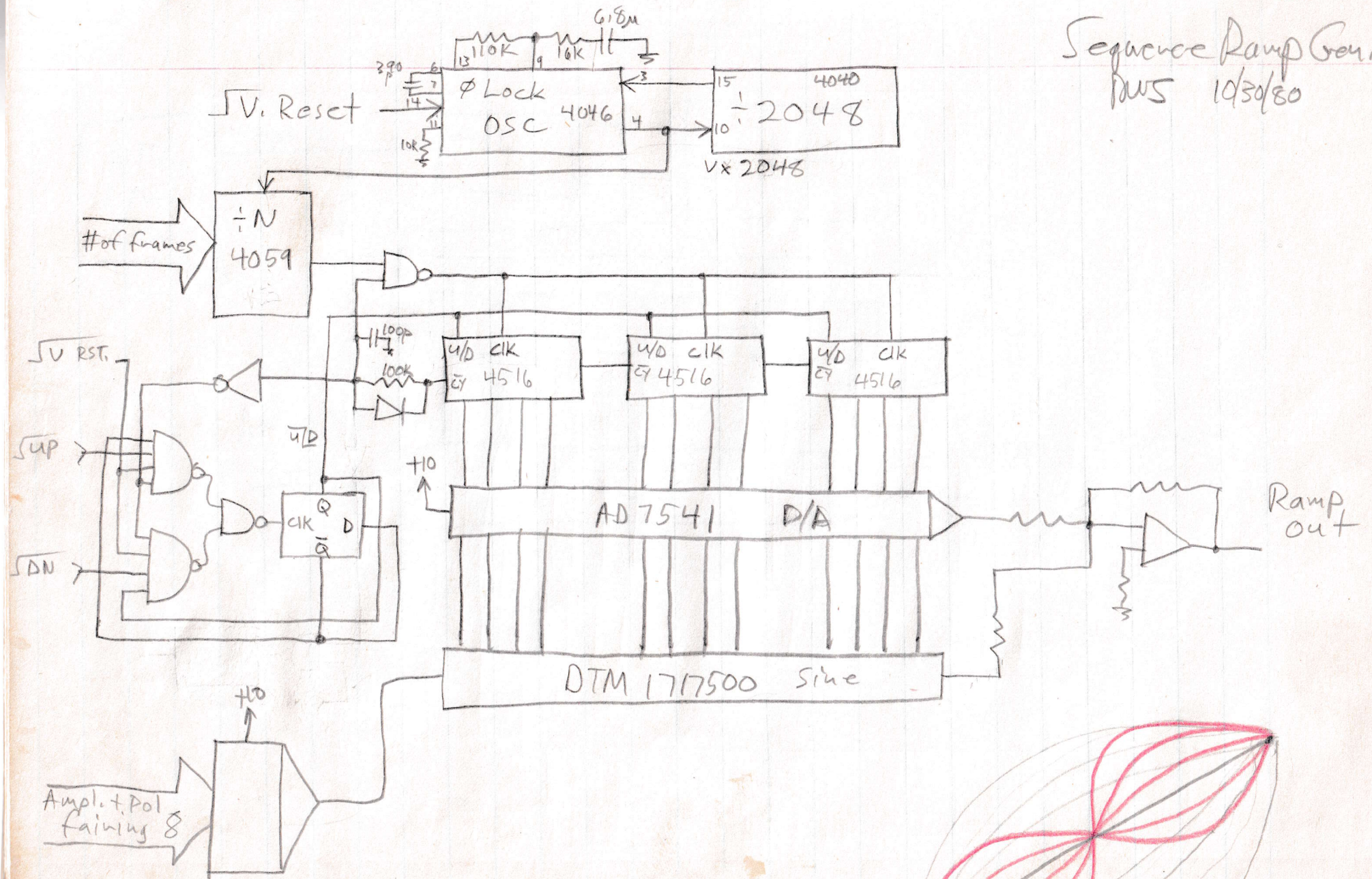
Visi REF  
ROSSA LCH  
ADD



Background Input

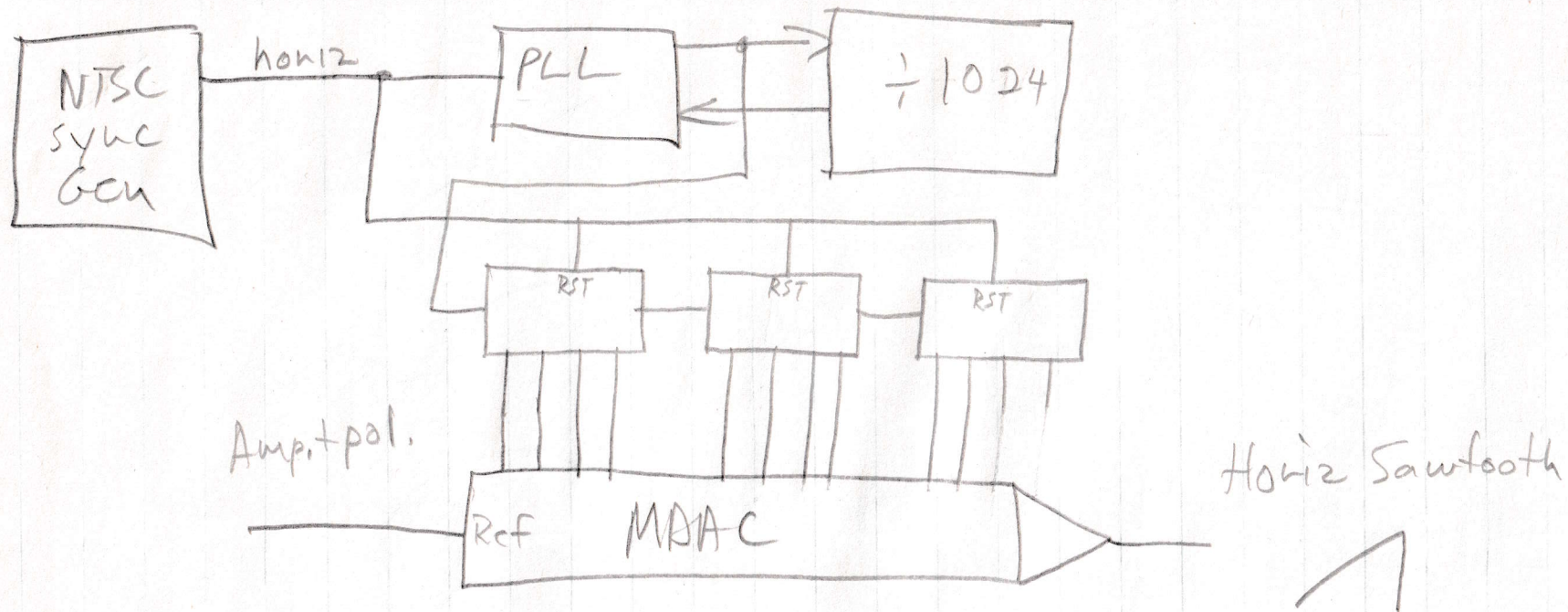


Sequence Ramp Gen.  
 PWS 10/30/80

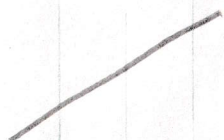
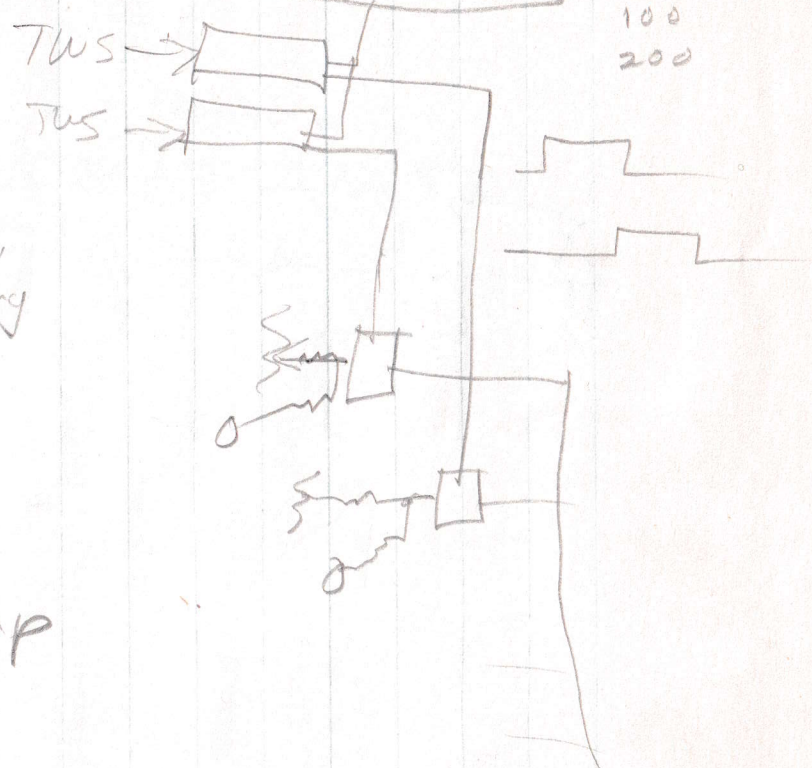
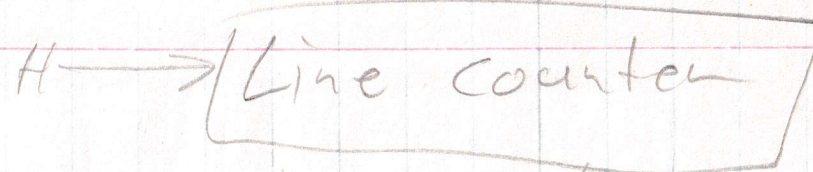




16.128 MHz







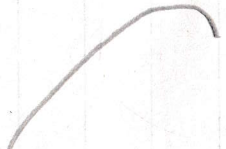
Ramp



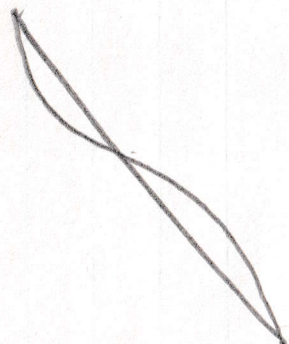
Ramp w/ falloff



Swoop



Swooped ramp



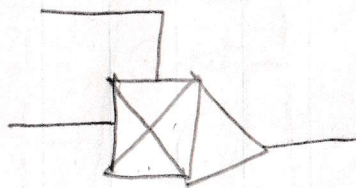


$\pm 10$

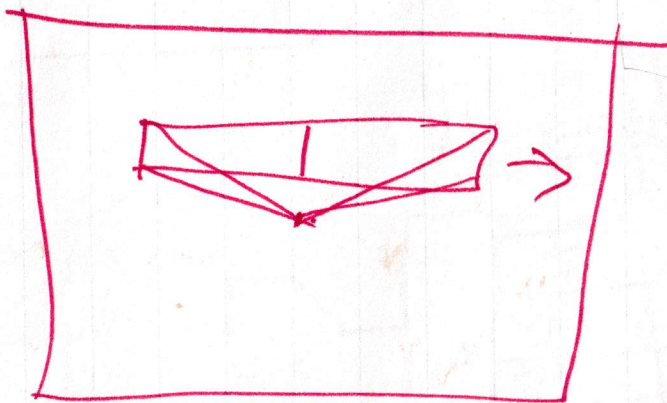
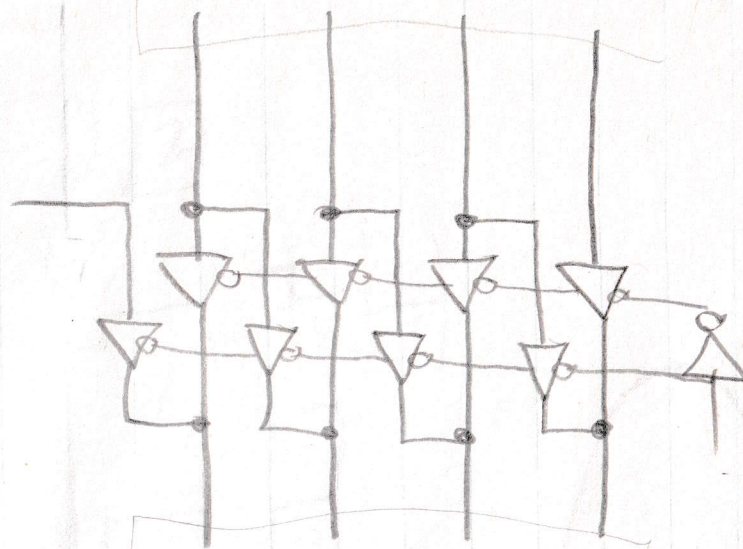
X

$\pm 10$

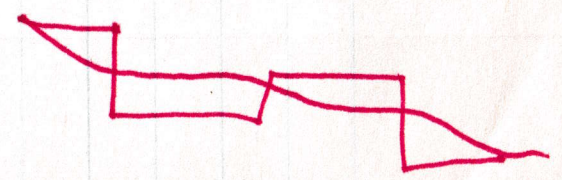
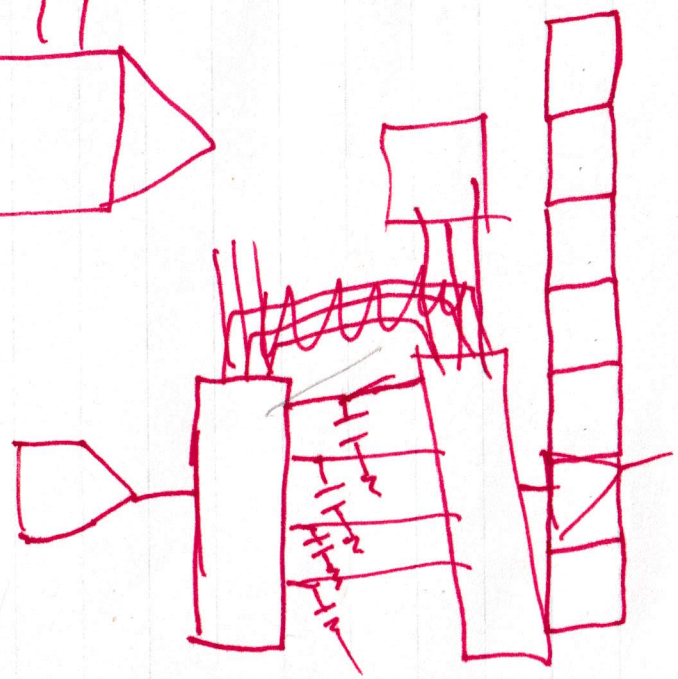
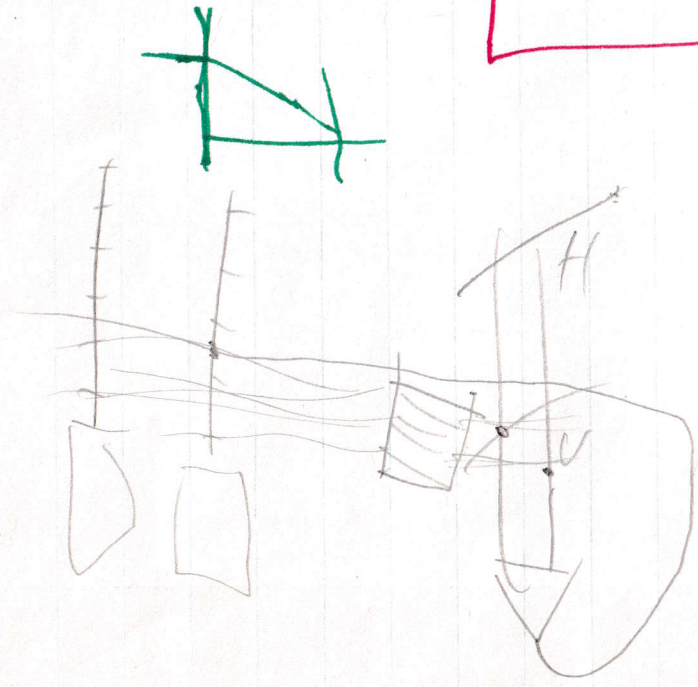
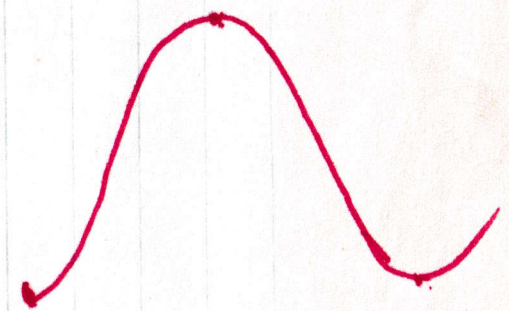
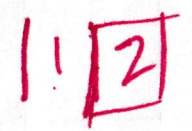
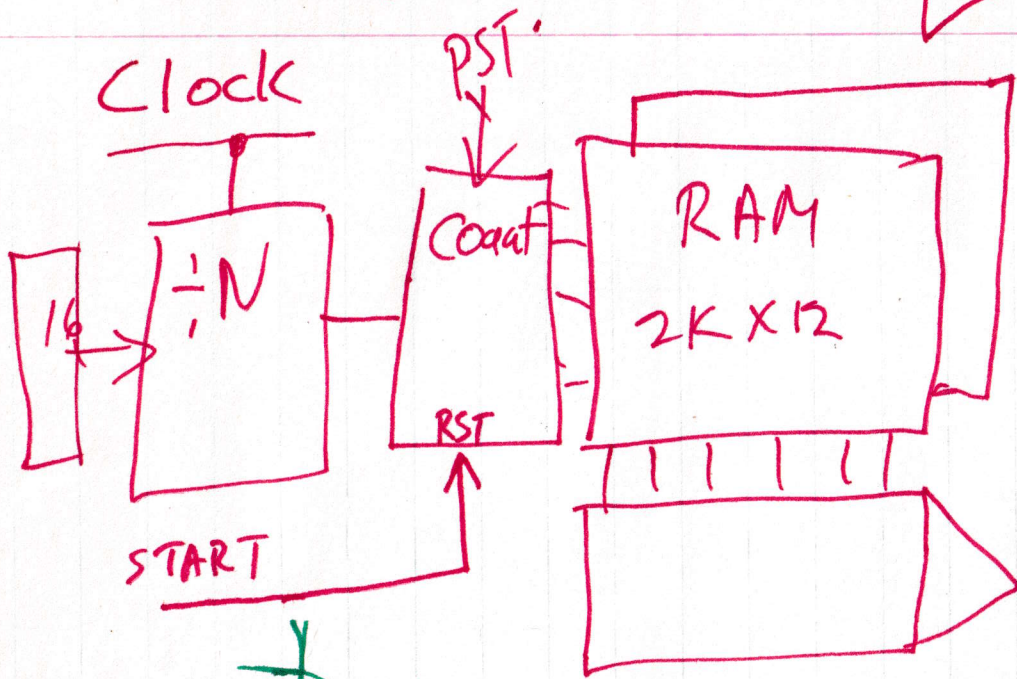
Y



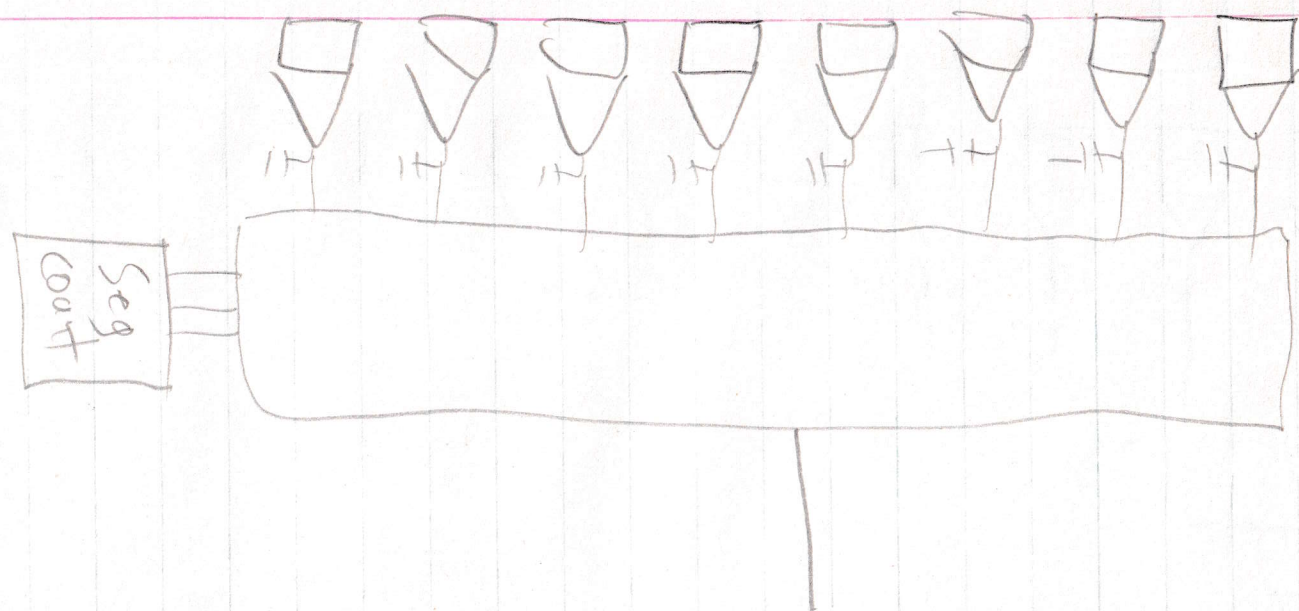
10



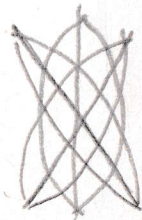
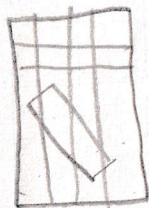




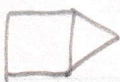
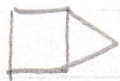
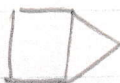
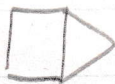
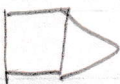
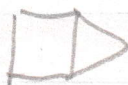
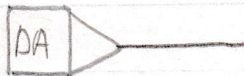
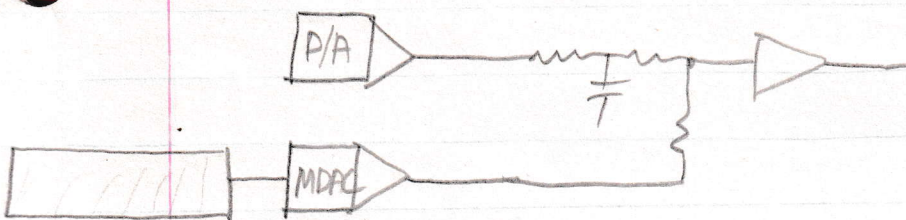




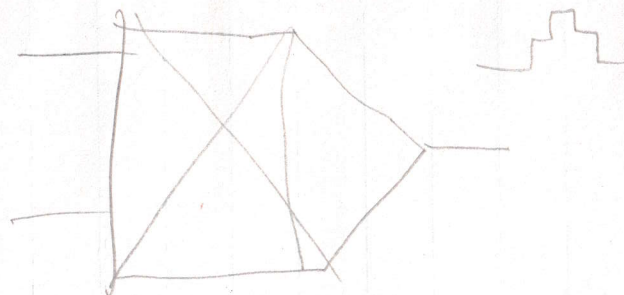
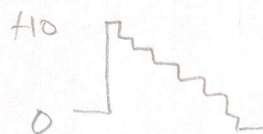
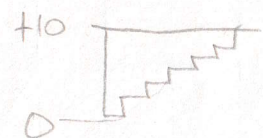






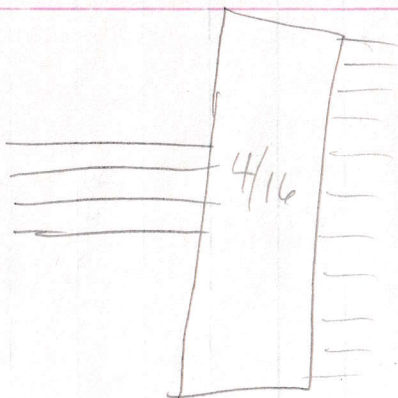




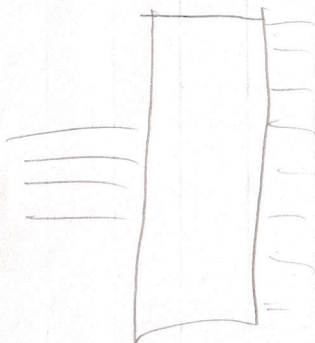




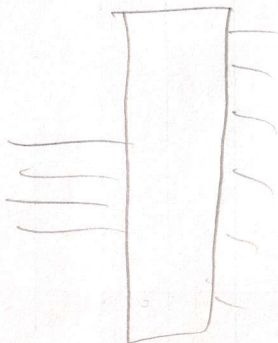
STST  
PRIO  
Dev 1



SYS  
PRIO  
Dev 2

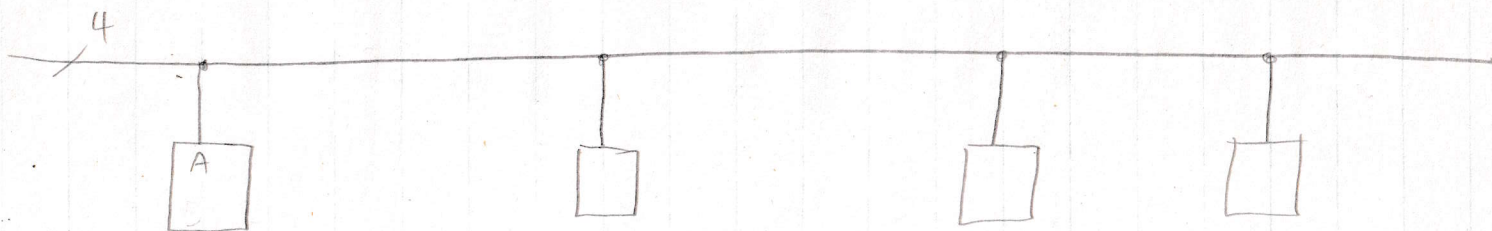


SYS  
PRIO  
Dev 3





Dev 1





80mm =

.0125

S	S'	M	
140 <sup>(5.5)</sup> mm	186 <sup>(7.323)</sup>	1.3	.007143
127	216	1.7	.007874

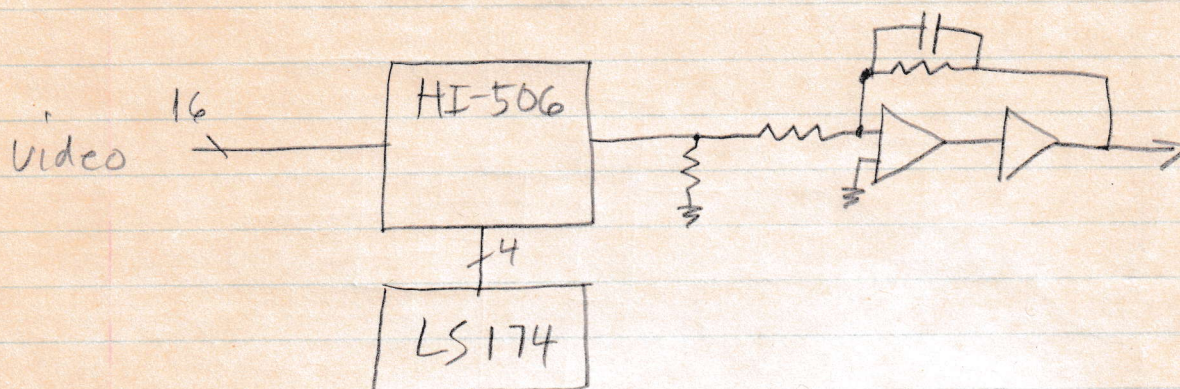
75mm = .013333

127 mm (5")	183 (7.2)	1.4	.007874
130 <sup>5/8</sup>	177 7"	1.36	.007692
132	173.6	1.315	.007575

70 mm



## Video coating

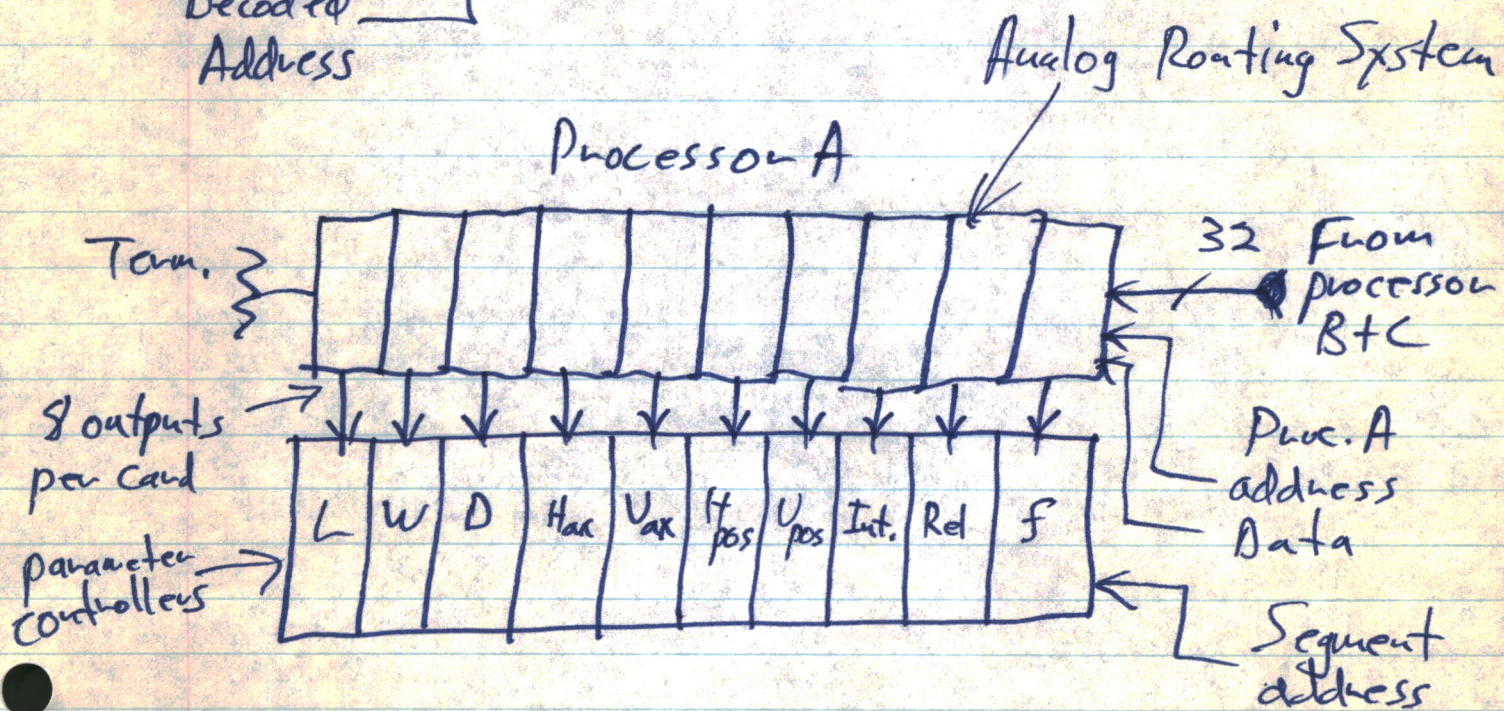
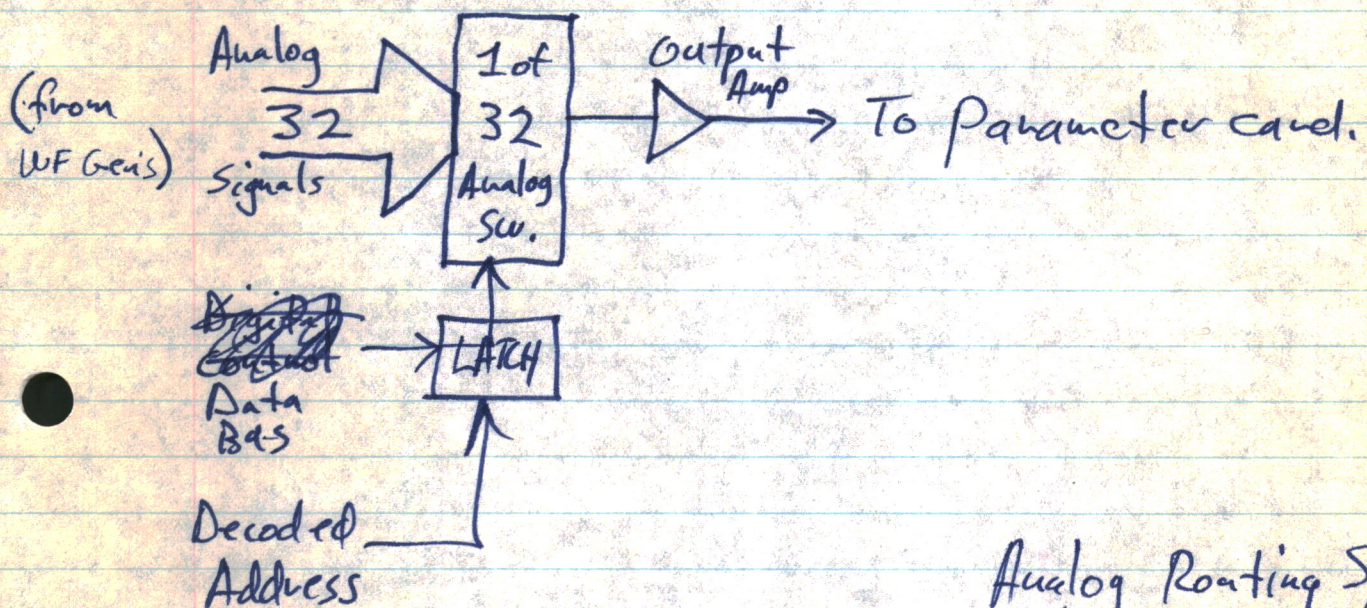


Per Card:



# Analog Routing System:

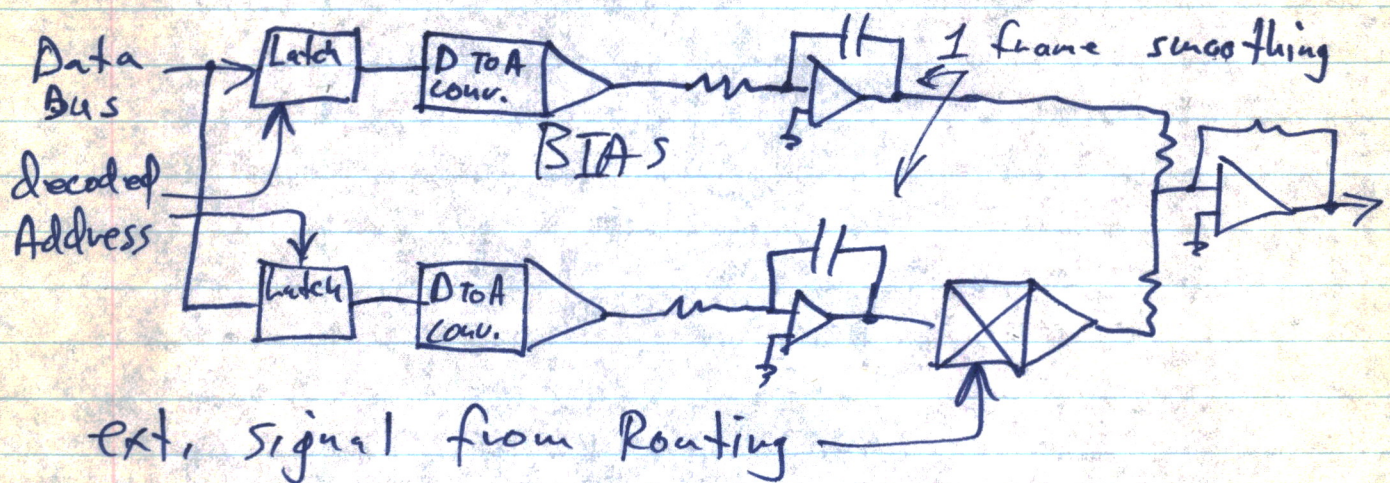
Function: To act as a wideband switching matrix. Each Analog Parameter <sup>controller</sup> ~~processor~~ requires <sup>such</sup> a ~~routing~~ matrix for selection of one of 32 analog sources





## Parameter Controller:

Function - to provide segmented control over one of ten analog parameters, per parameter, per segment each controller looks like this:



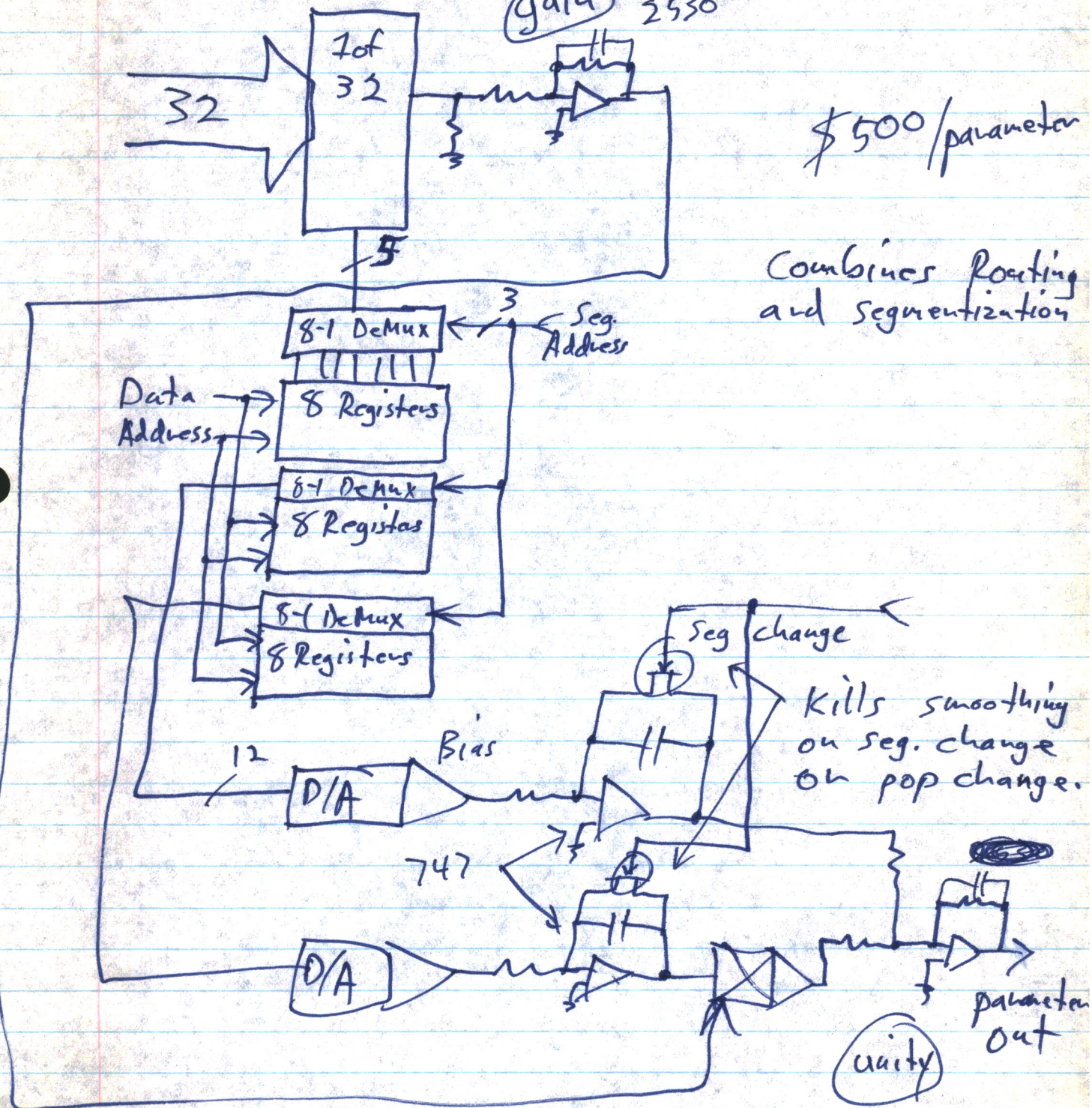


One possible alternative:  
Per Parameter:

gain 2530

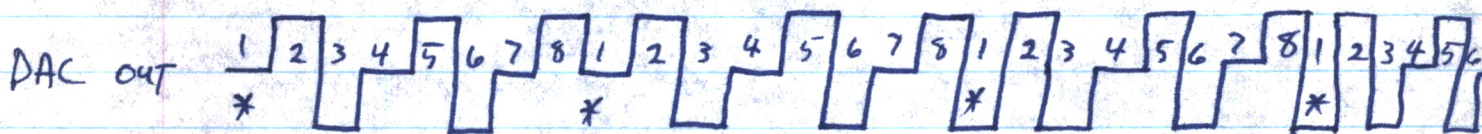
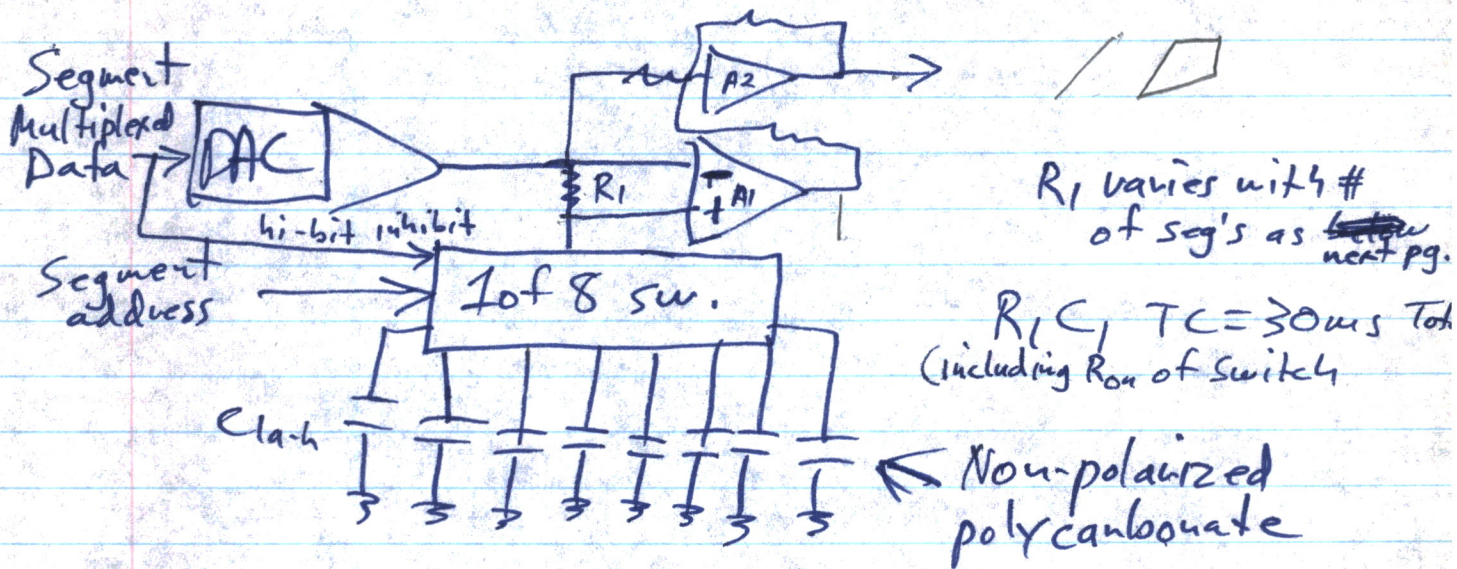
\$500/parameter

Combines Routing  
and Segmentation



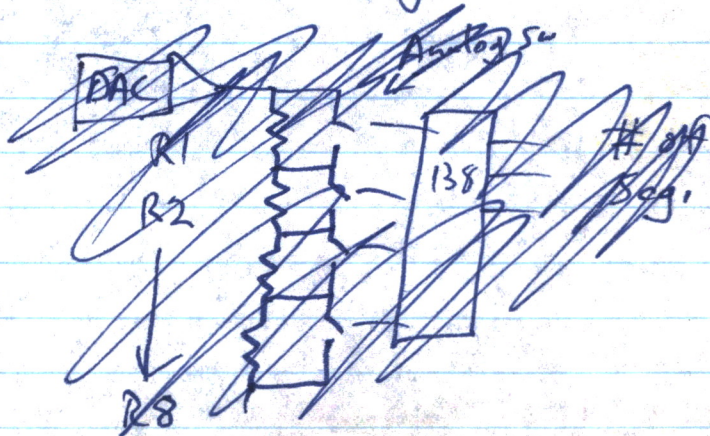
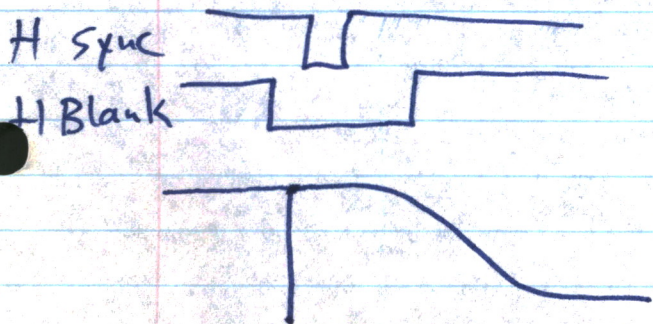


## An added note on Parameter smoothing



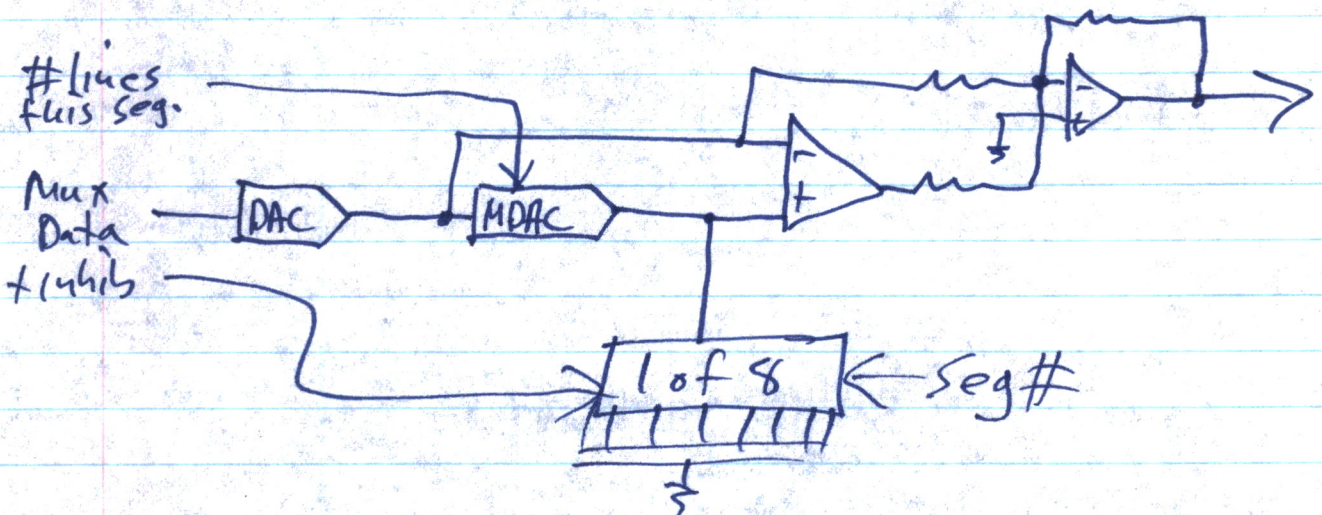
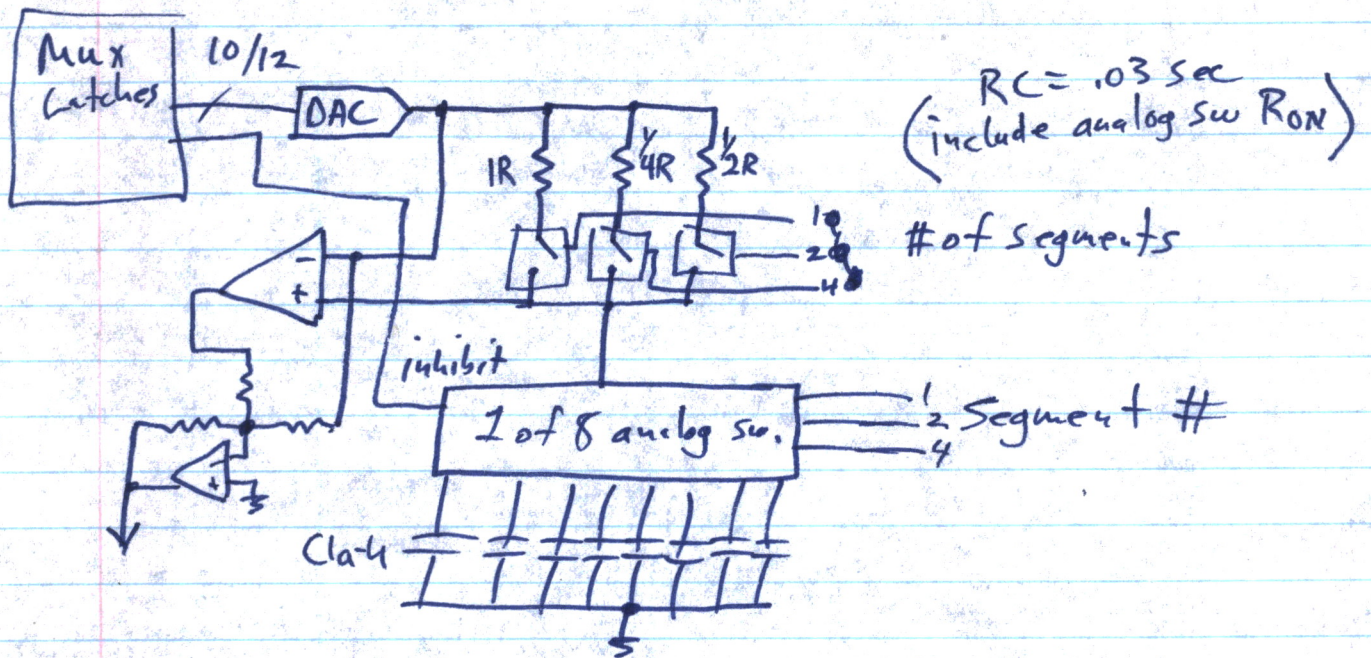
AI  
OUT (drawn invented)  
Apparent  
Seq 1

Segment address must change during Horiz blanking and be settled and deglitched before unblank:





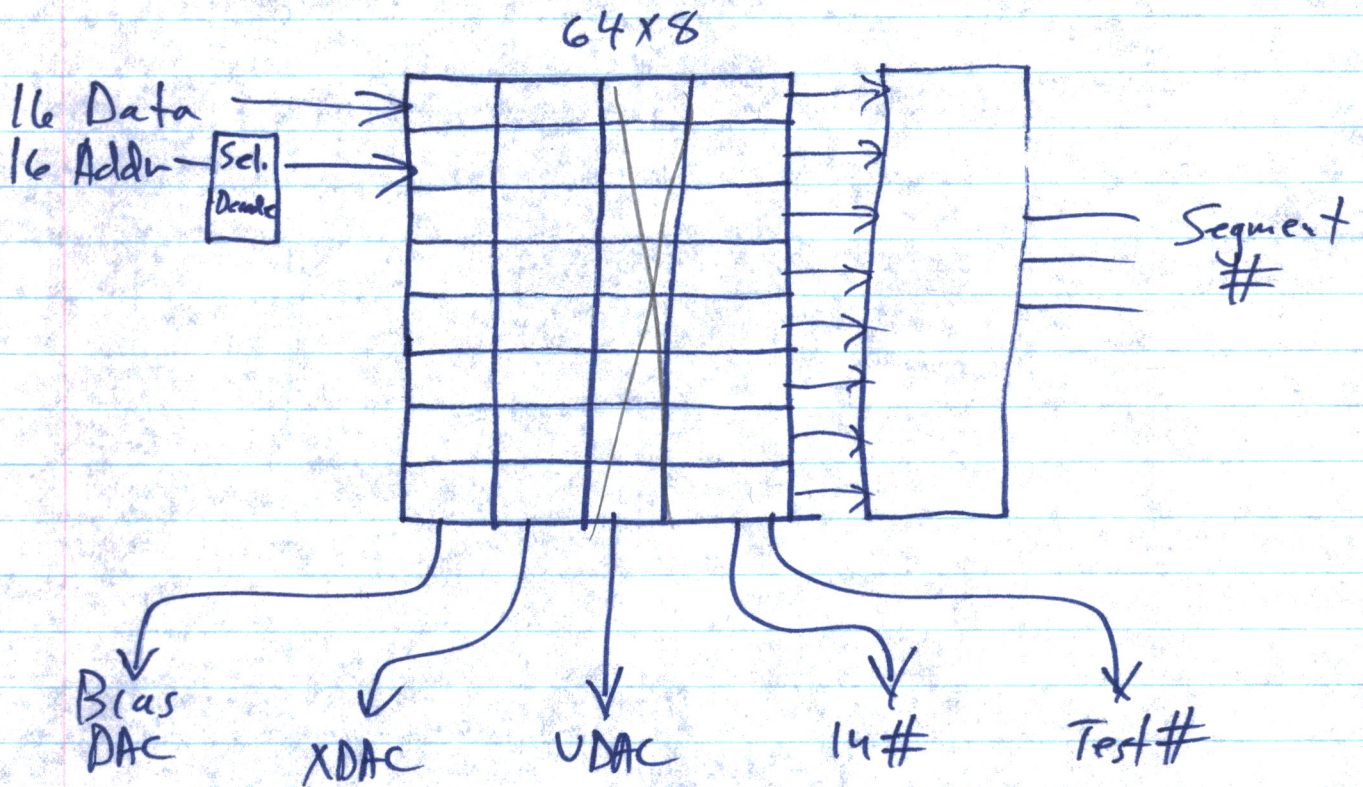
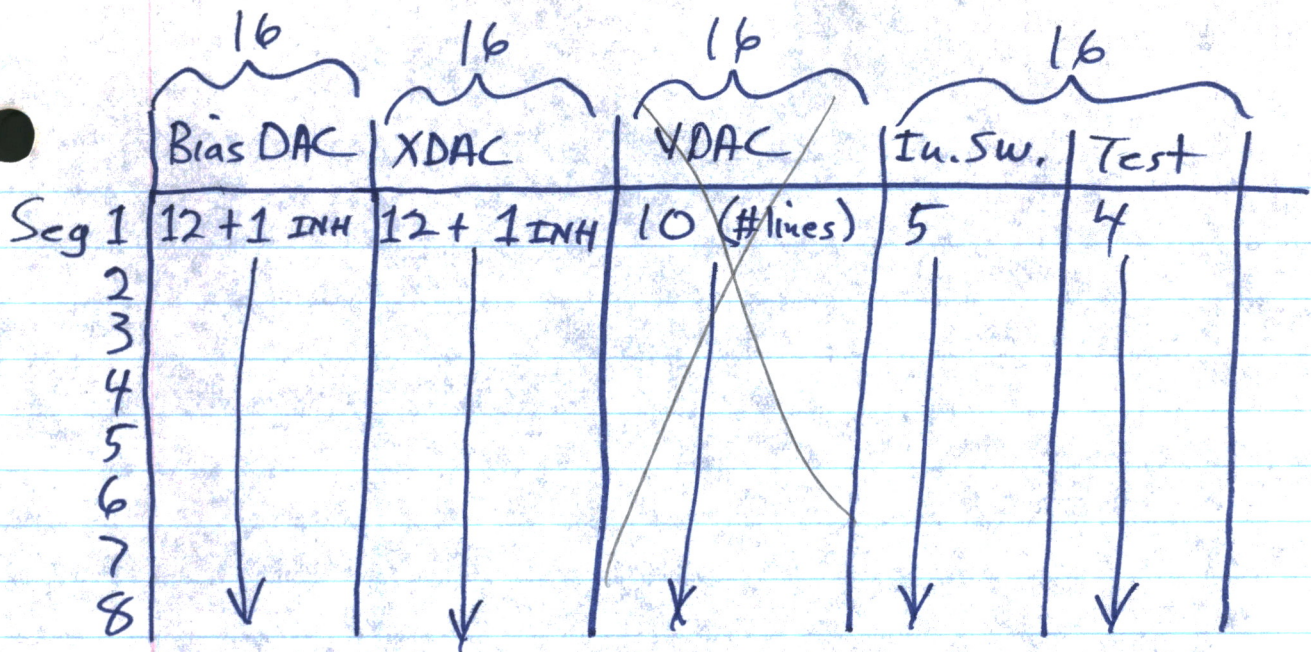
# Parameter Velocity correction;



## Per Parameter card:

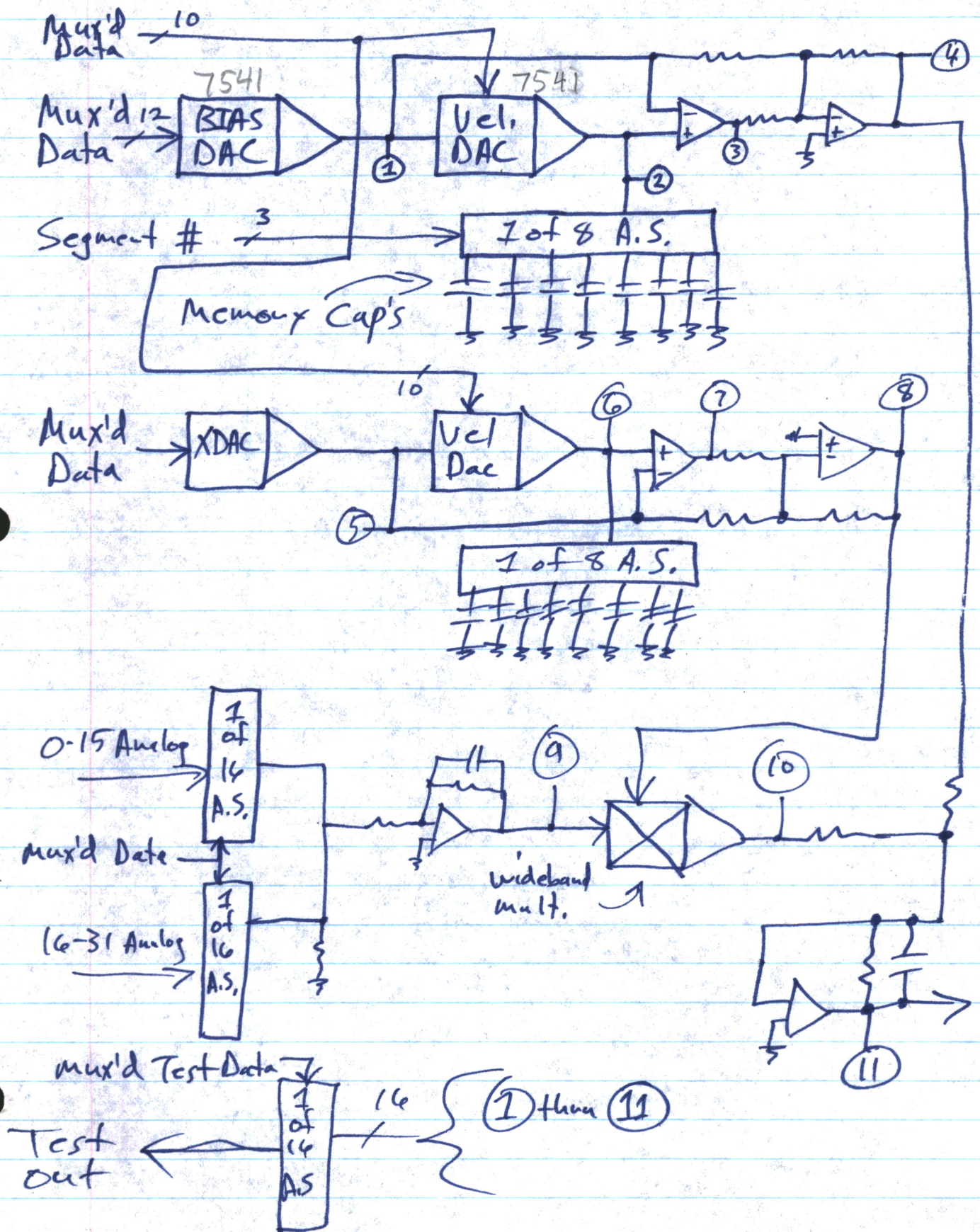
- 5 bits x 8 seg - which of 32 Analog inputs
- 10 bits x 8 seg - bias
- 10 bits x 8 seg - ext multiply
- 10 bits x 8 seg - #lines each seg - velocity
- 1 bit x 8 seg - accompanies bias + ext - 12.6 bits
- 3 bits - Segment # (not latched) velocity







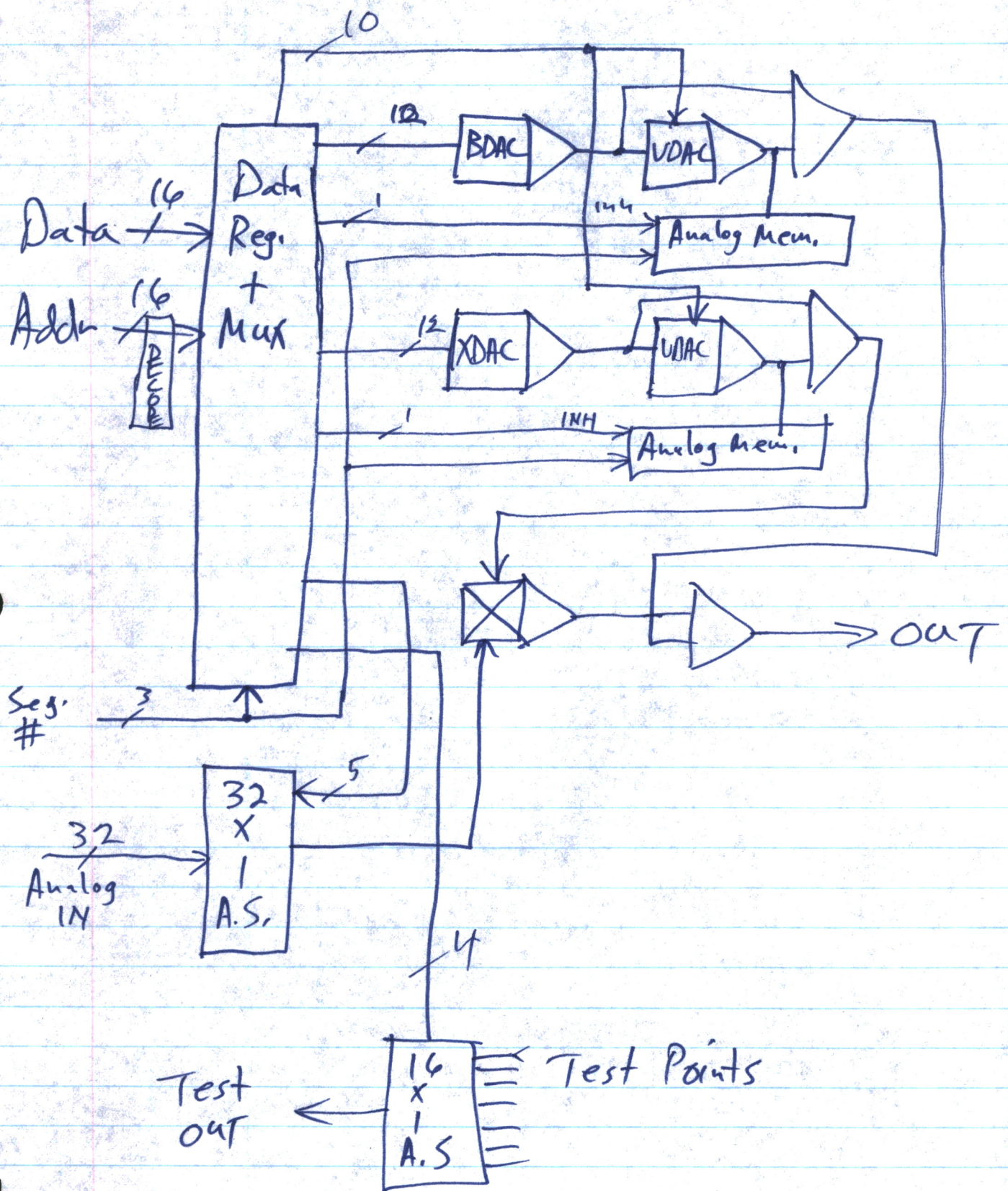
# New Parameter/Analog Routing



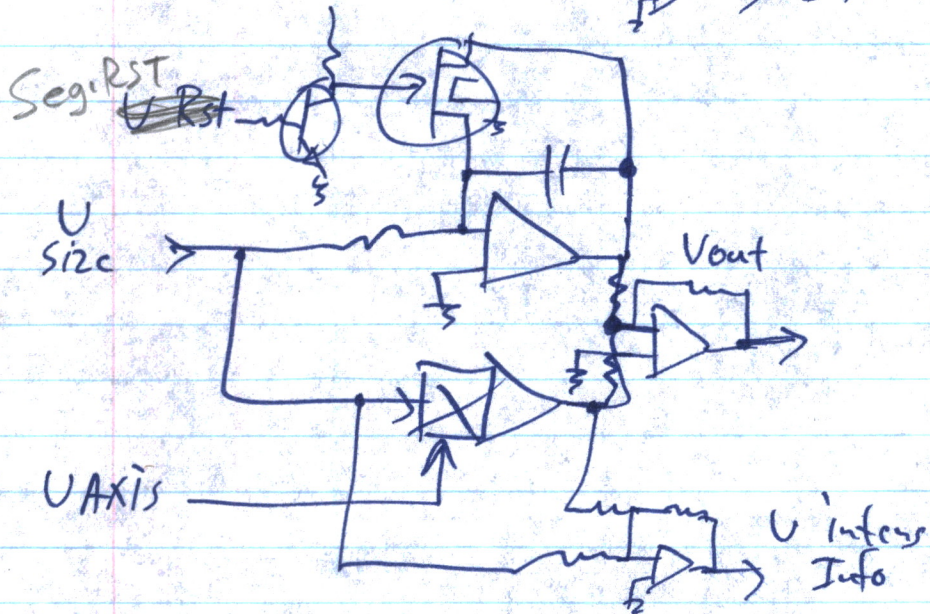
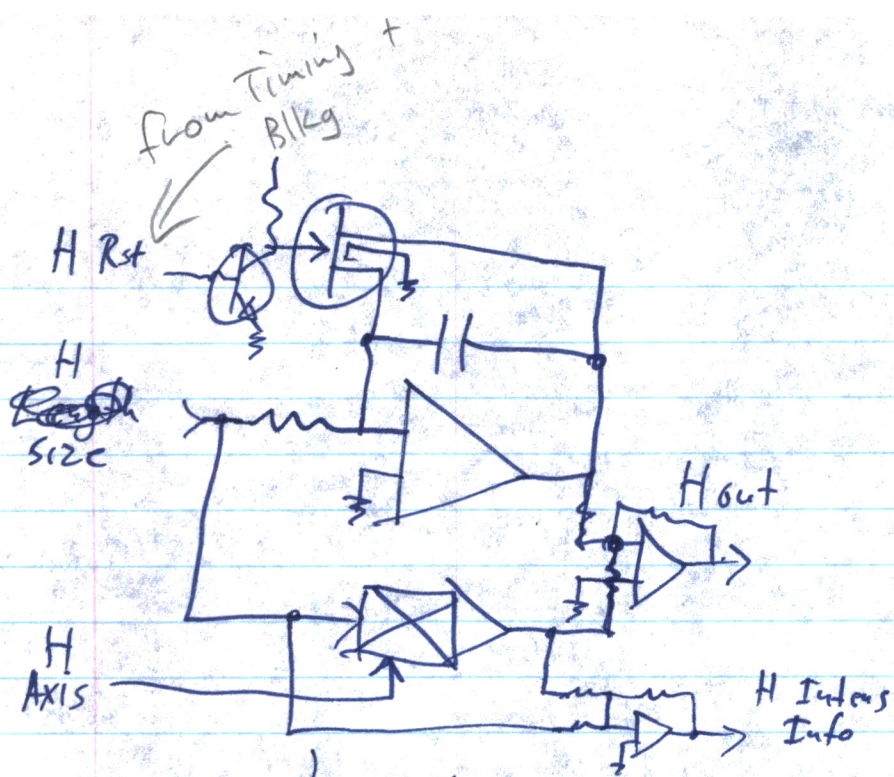








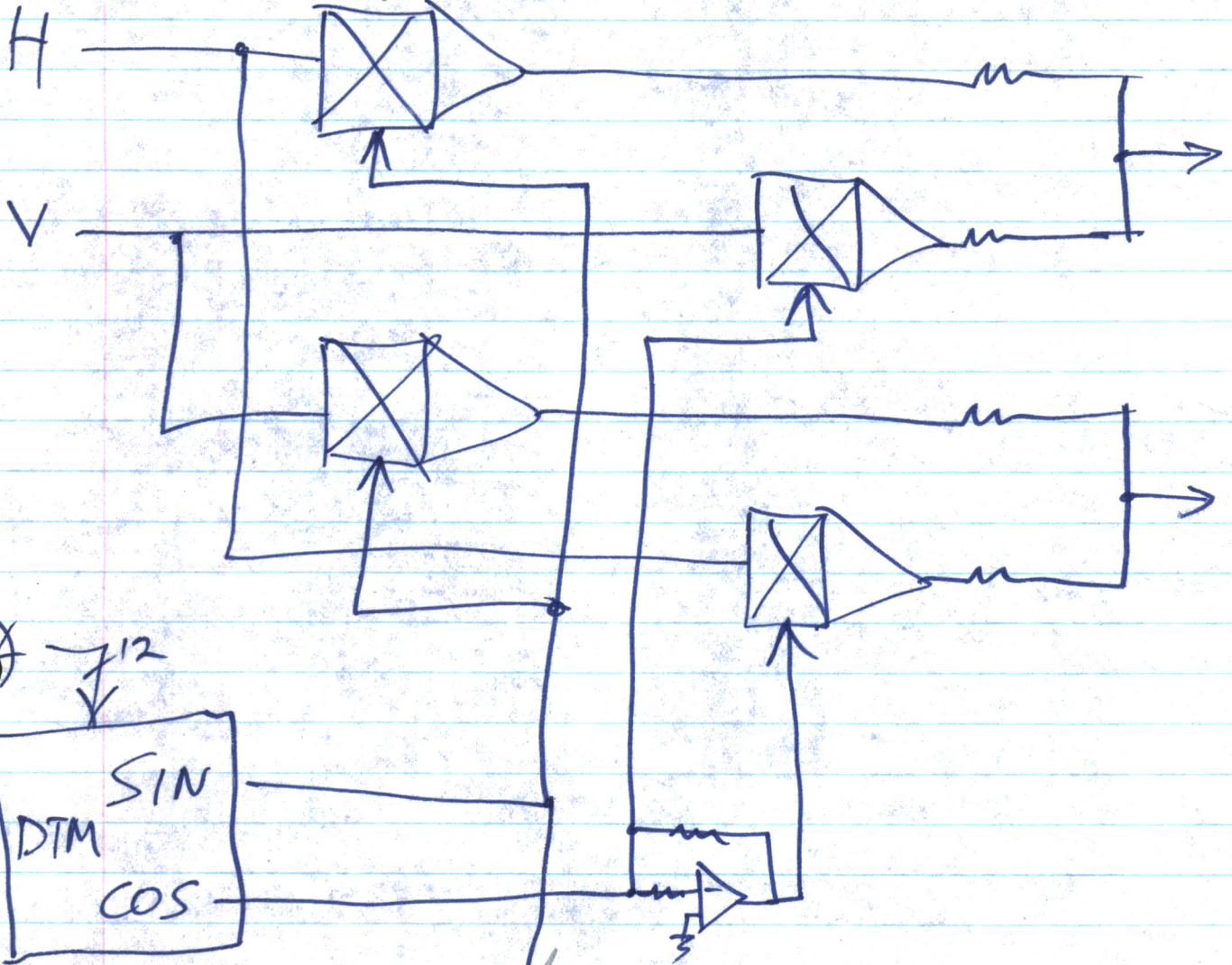






275 DTM/1217

429B-150

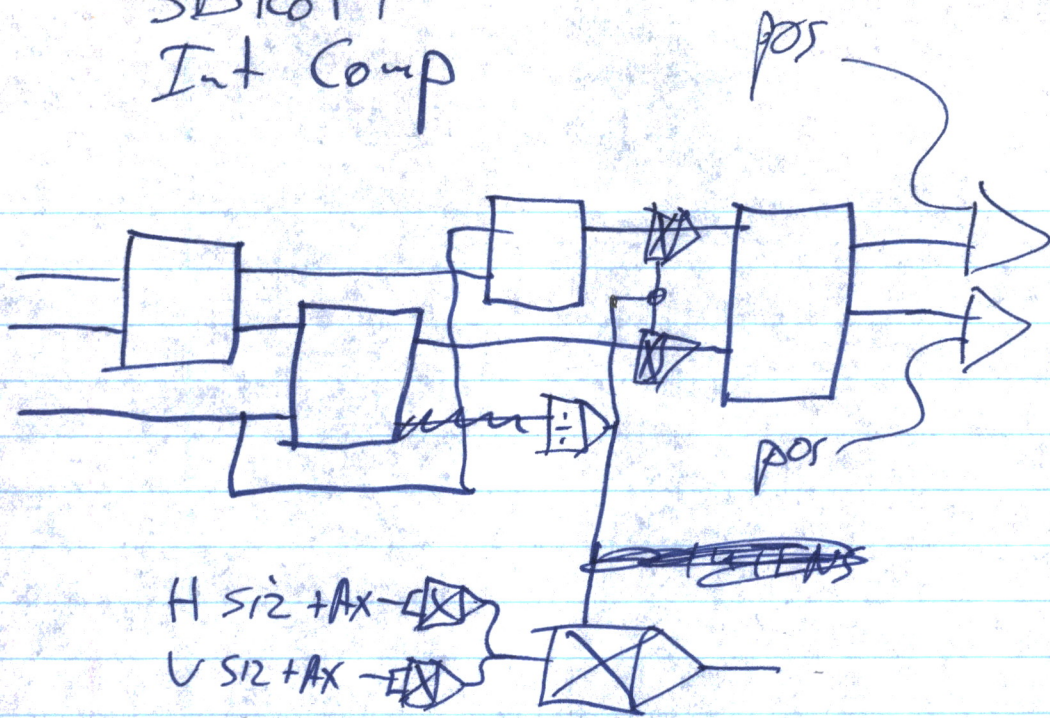


~~s~~  
~~c~~

~~429B-150~~ → Rot + Vcl. ?



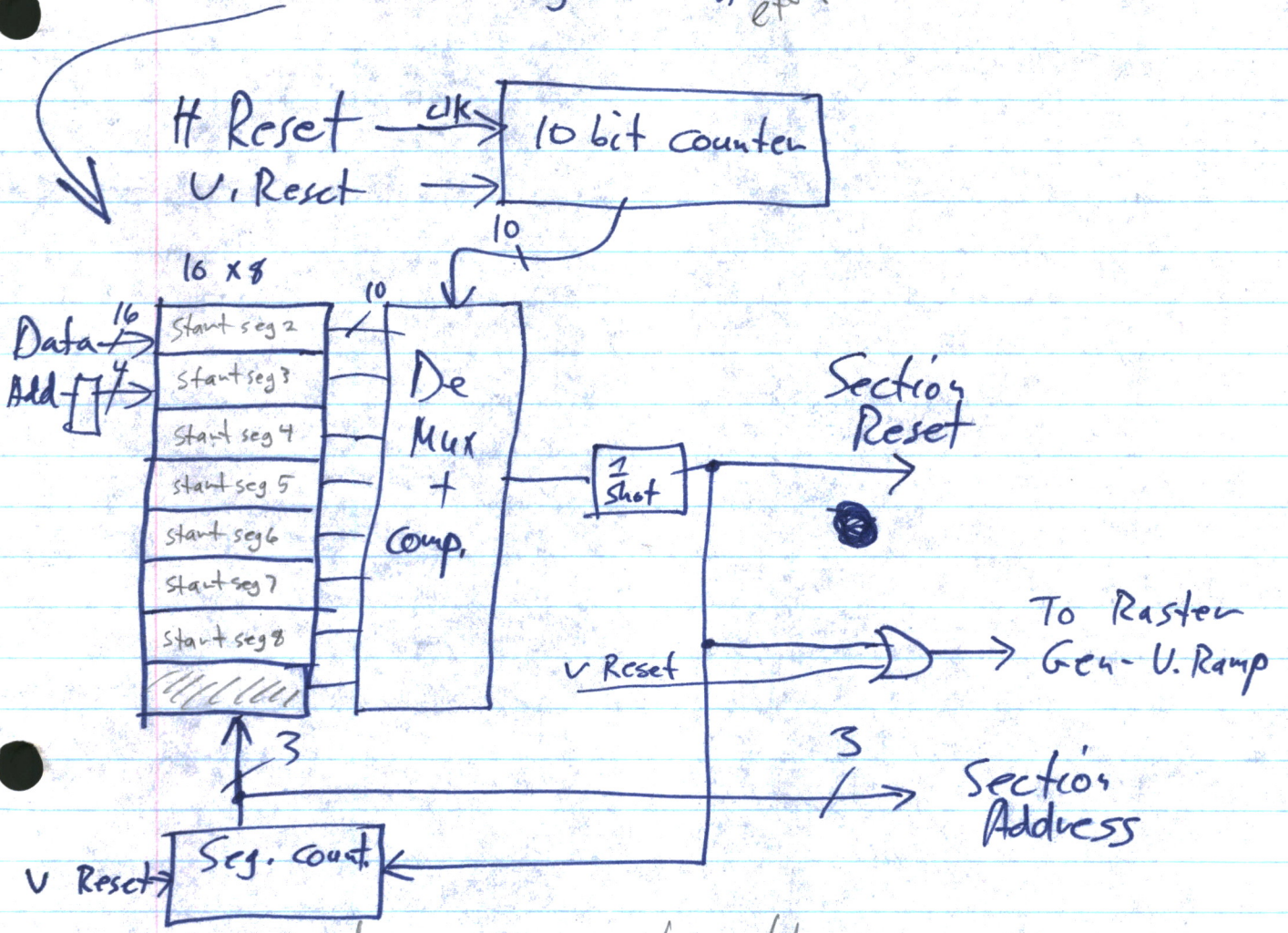
# 3D Rot + Int Comp



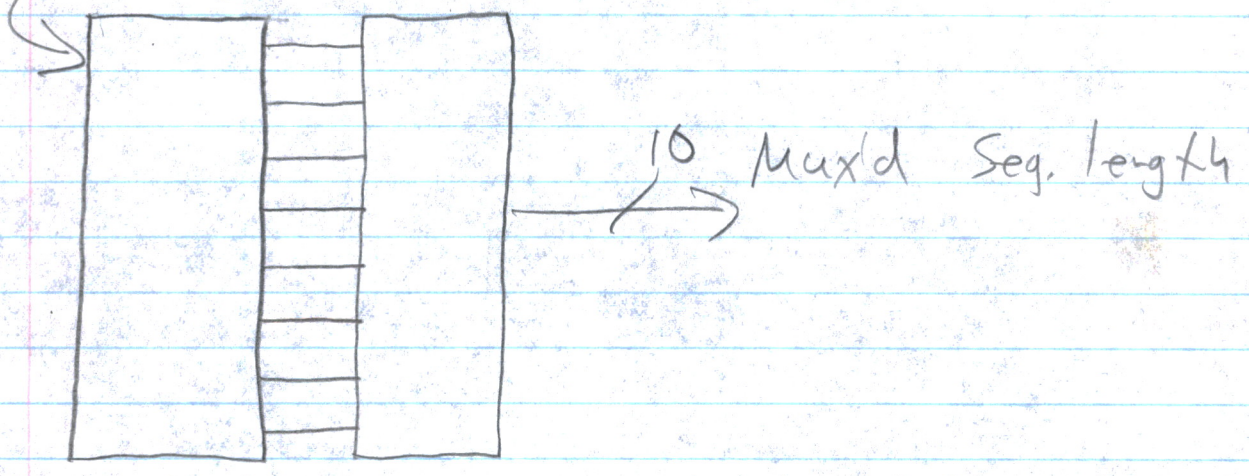


# Seg. Control

Data = Starting Line # <sup>except seg 1</sup>

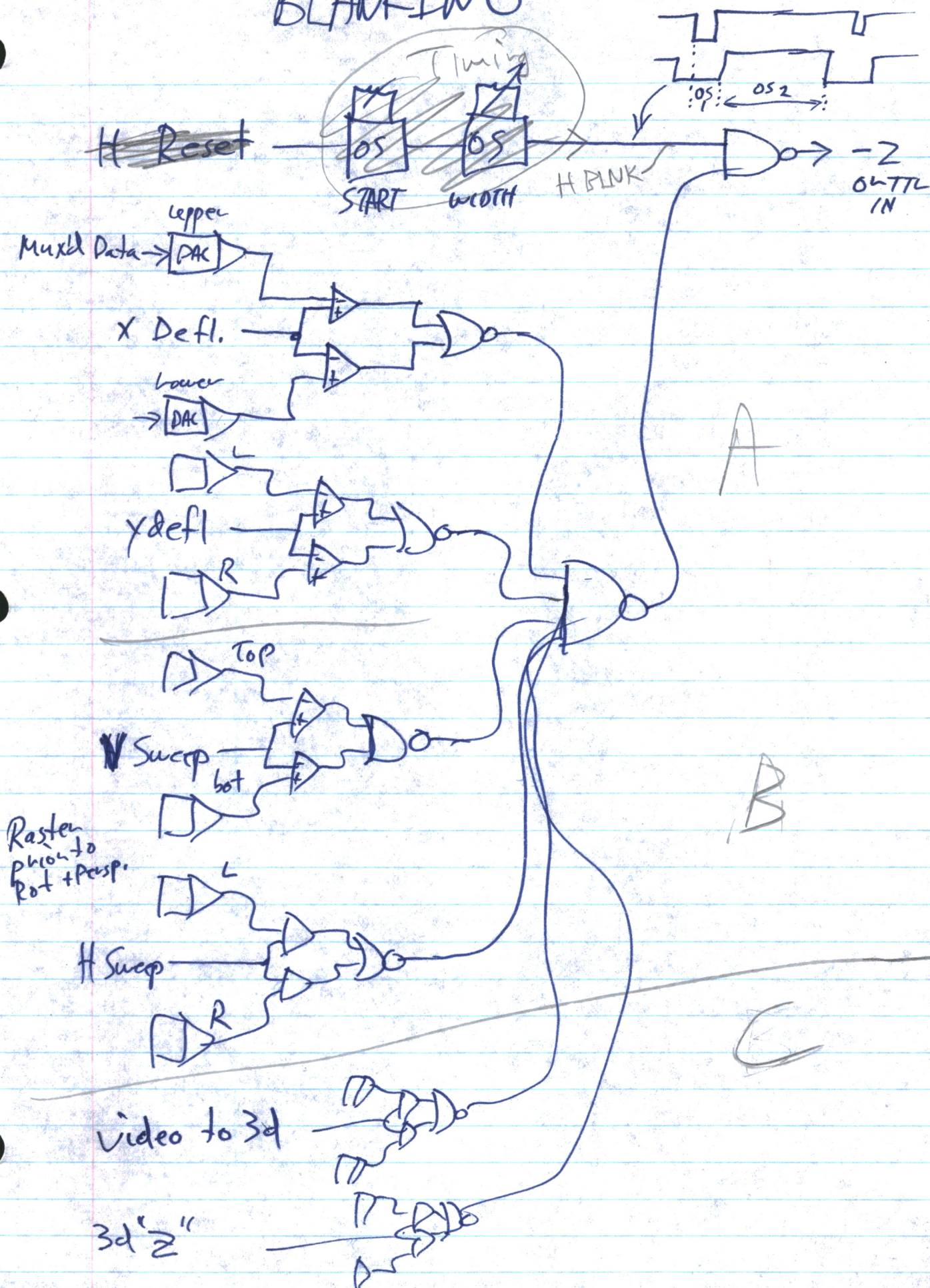


Data = Seg. length



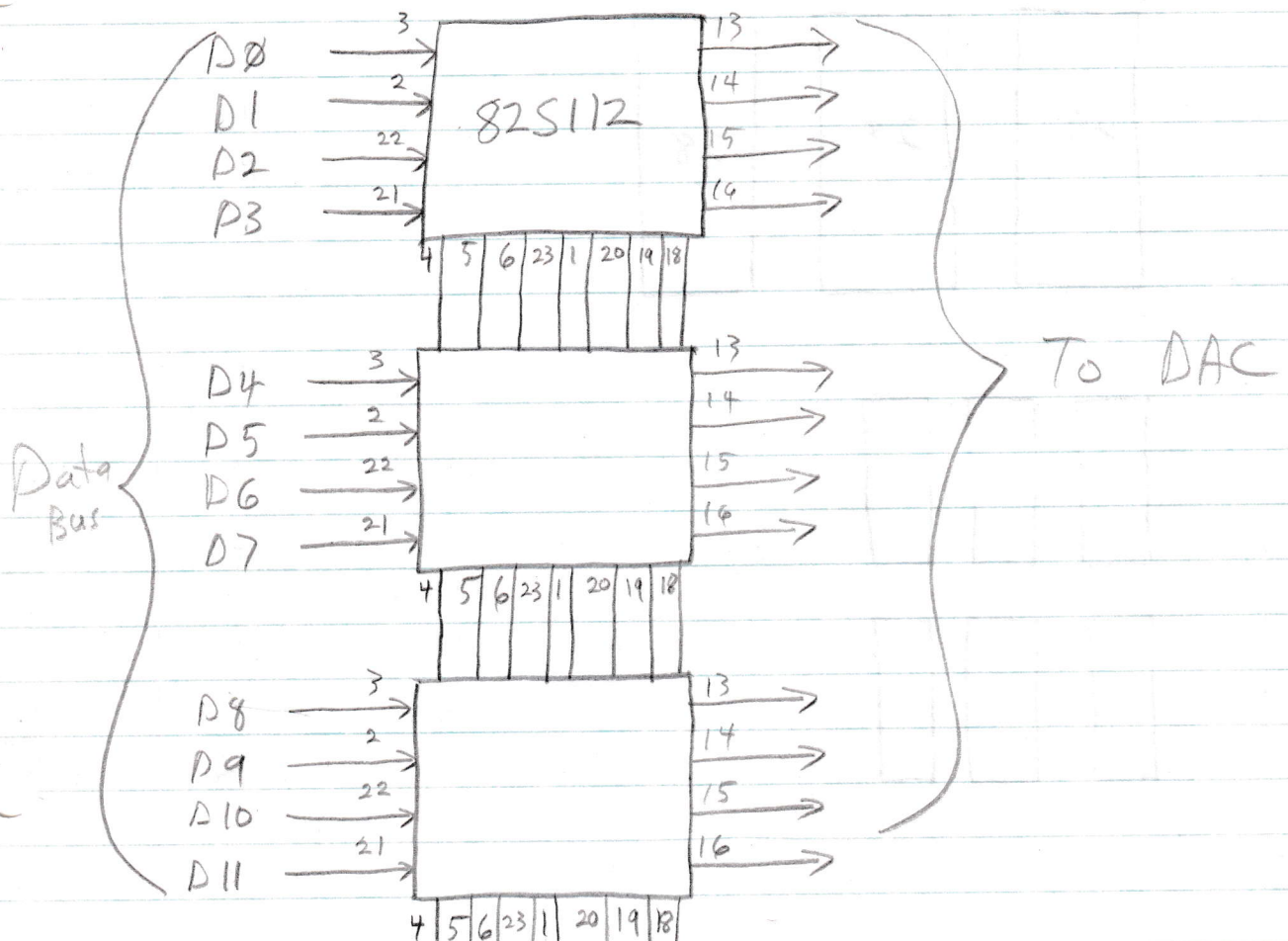


# BLANKING

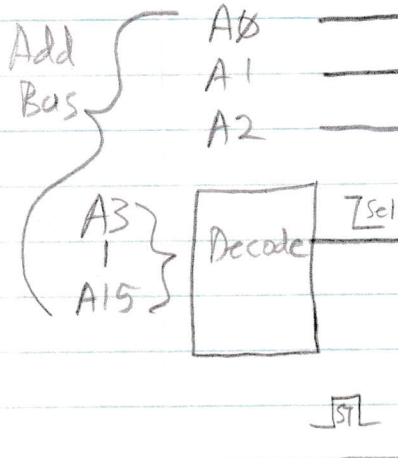




All pins 7 = hi



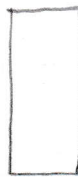
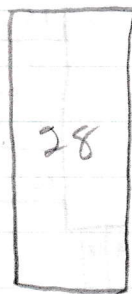
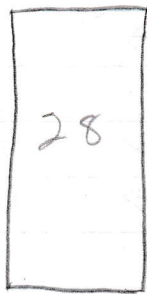
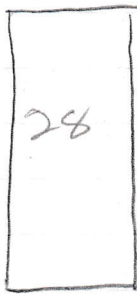
Pins 8, 9, 10, 11 = NC



0 1 2

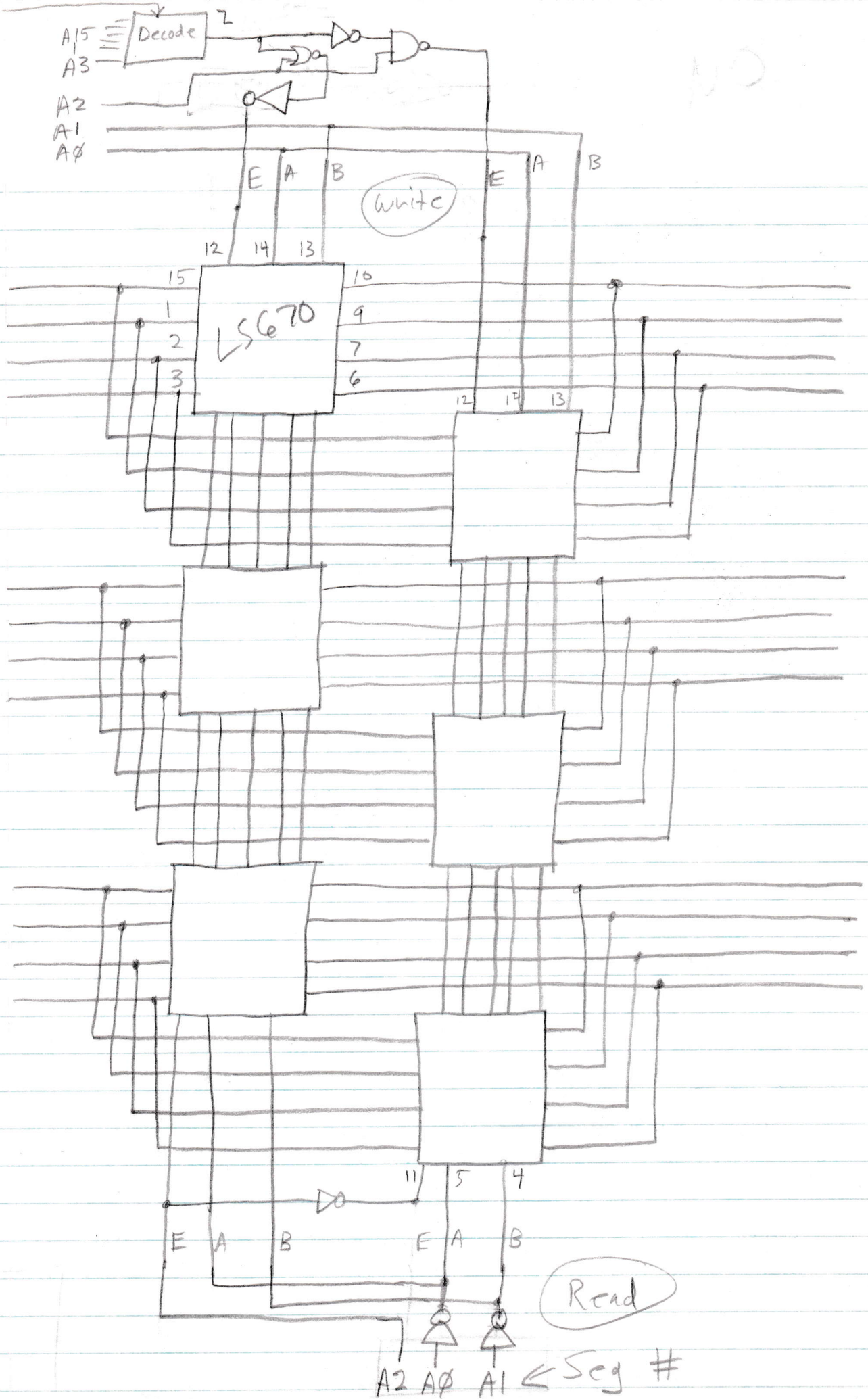
Segment #







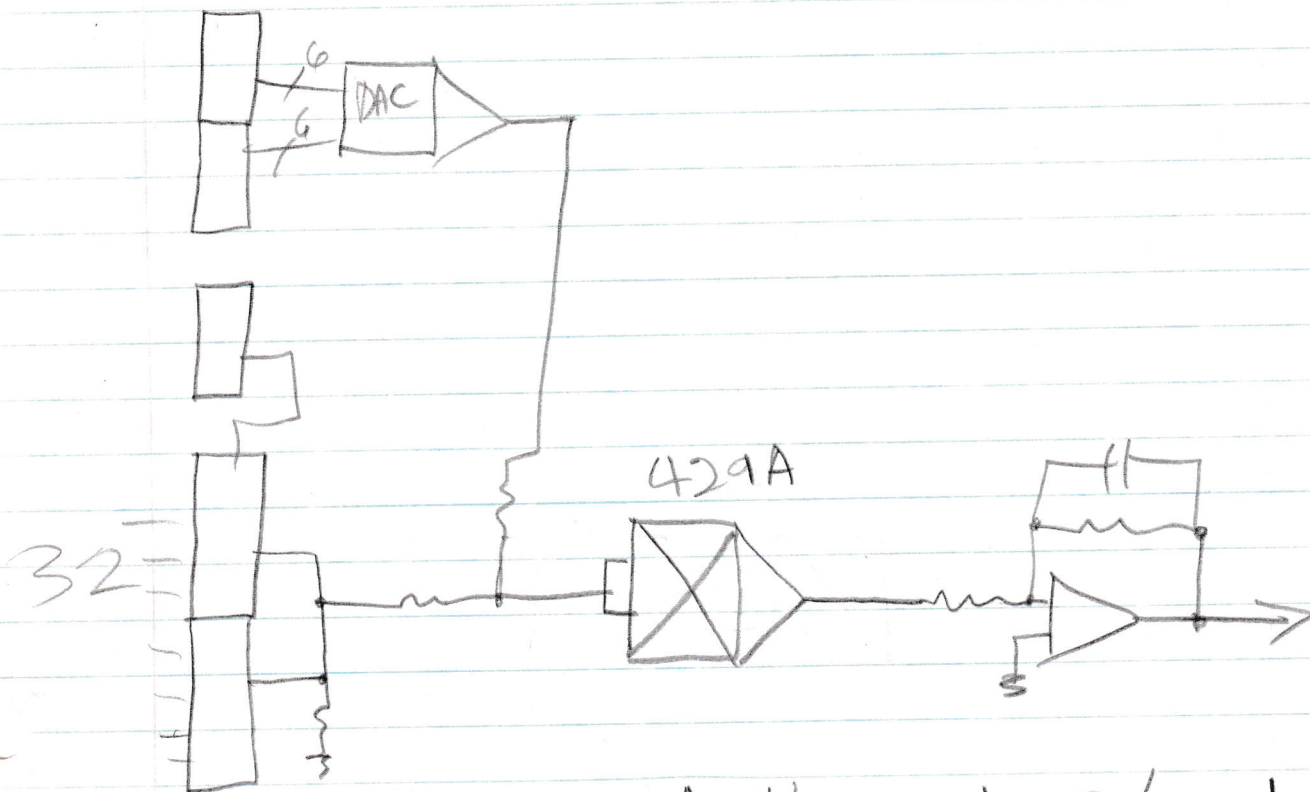
STR





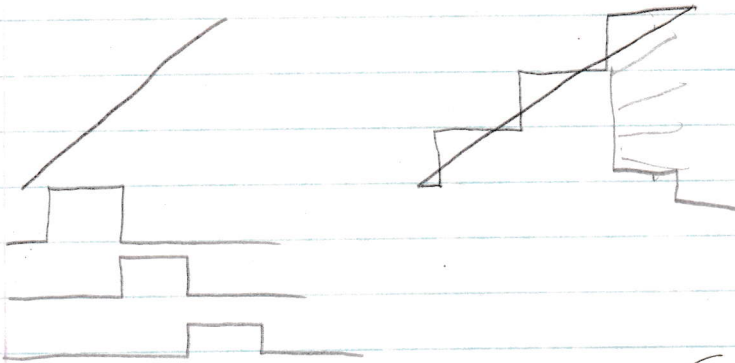




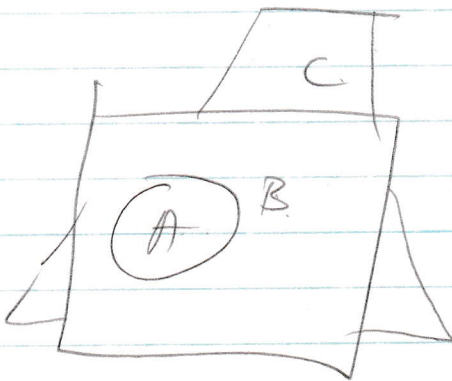
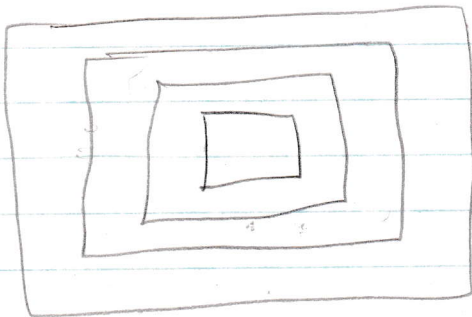


Mult. Card - 2/card.



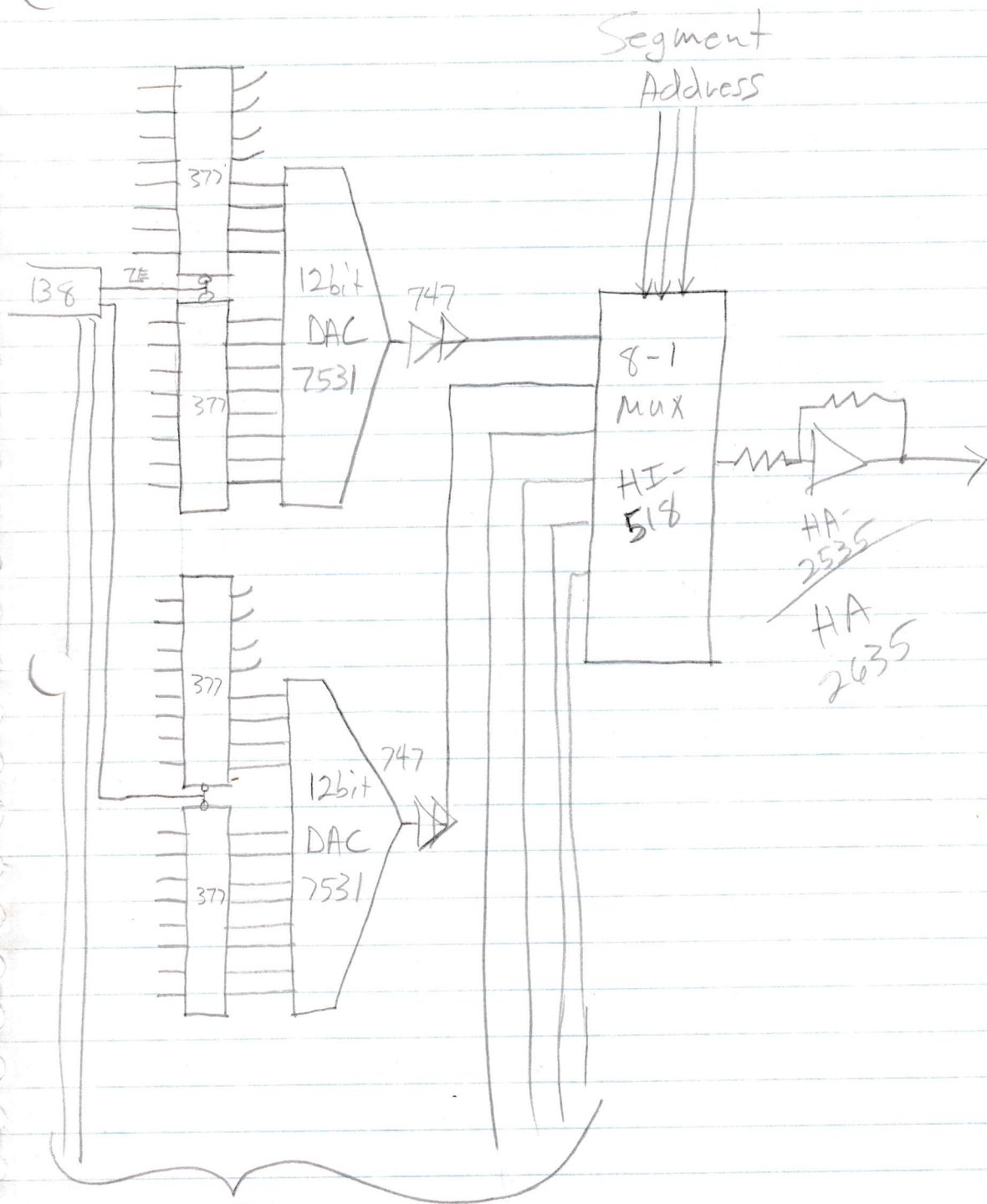


Set Gx levels  
Set RGB values  
Set RGB/Y Mix  
Set Audio level





# FLYING SPOT:

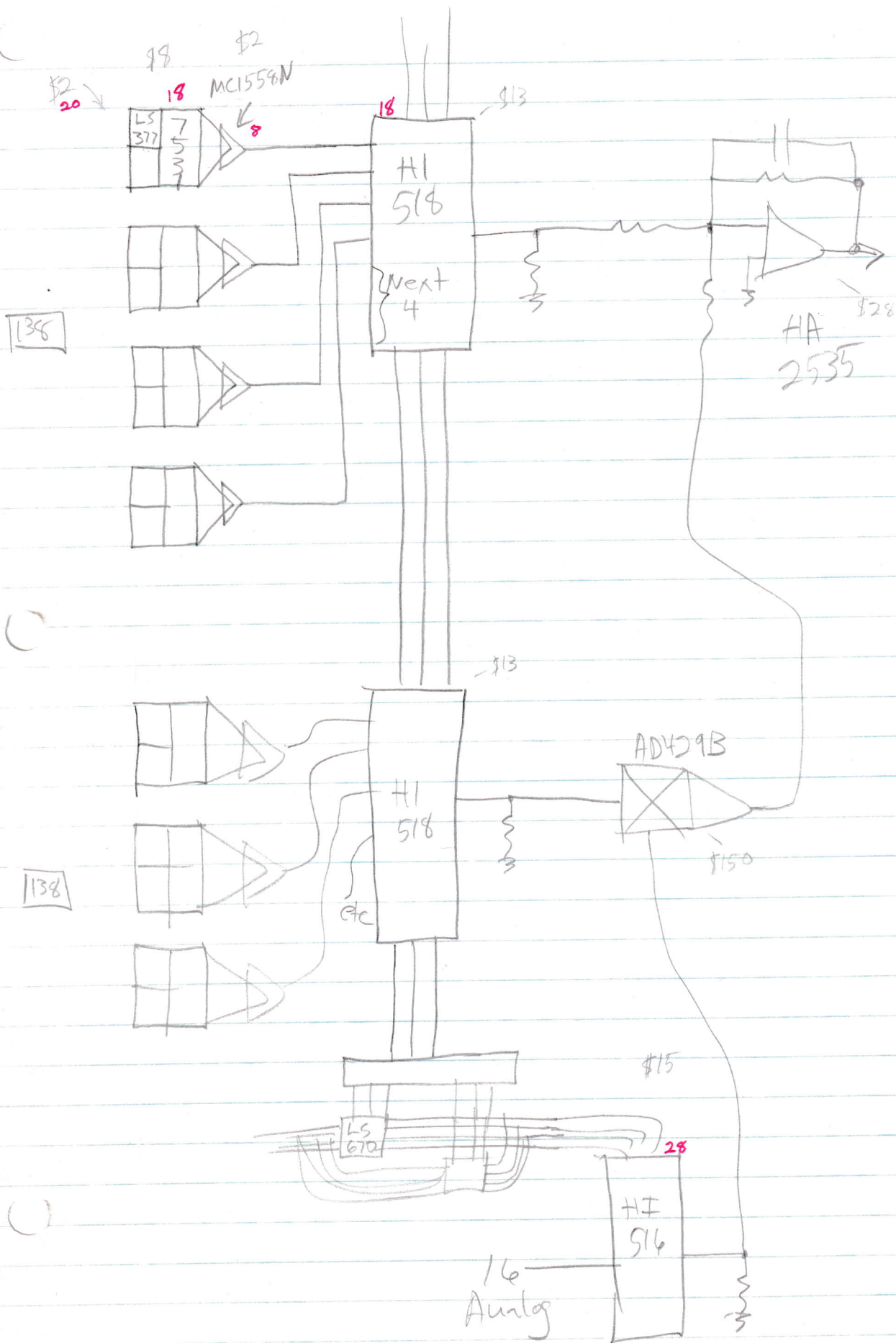


etc

$$\begin{array}{r}
 501.28 \\
 30.07 \\
 \hline
 531.35
 \end{array}$$



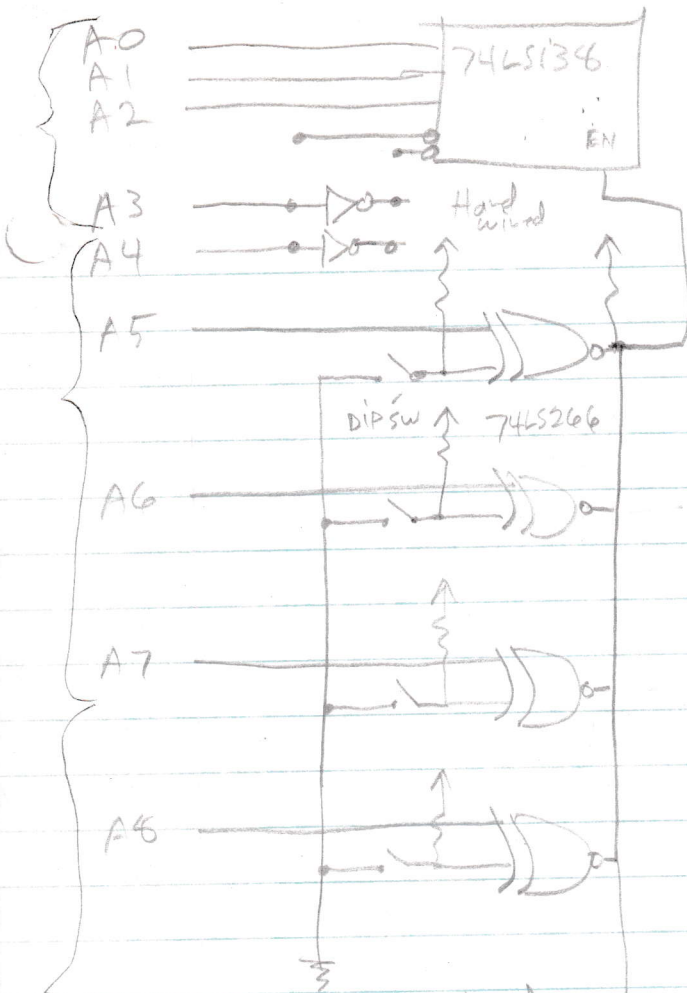
Seg Addr



14  
 x 32  
 448  
 + 26  
 474  
 + 150  
 524  
 15  
 639  
 28

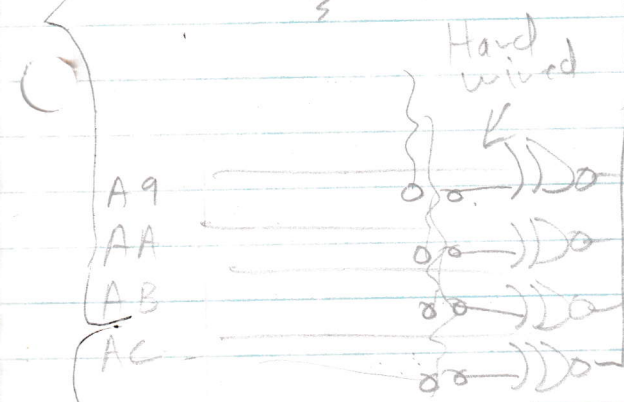






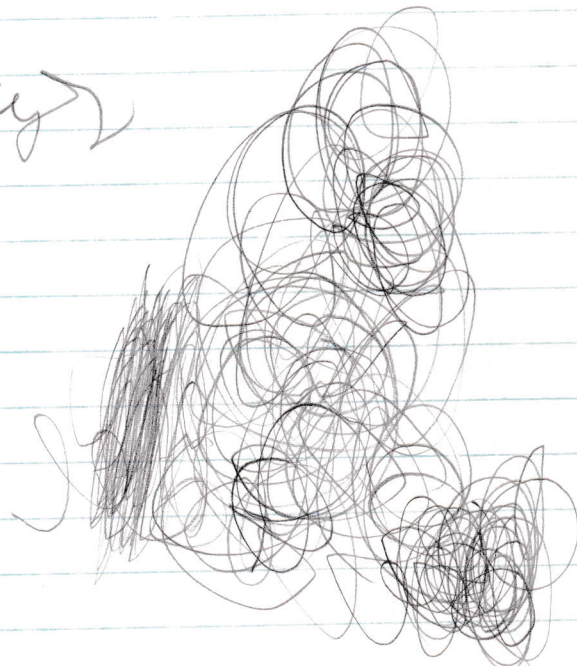
1 of 32 per board.

1 of 16 similar Boards

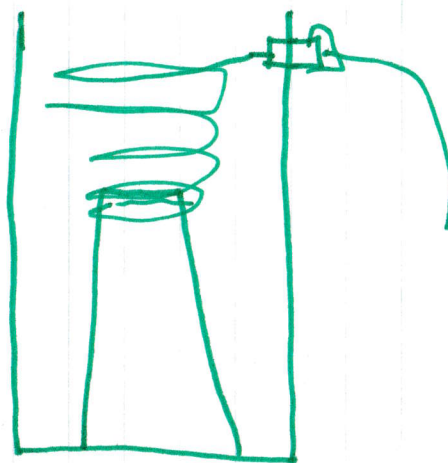
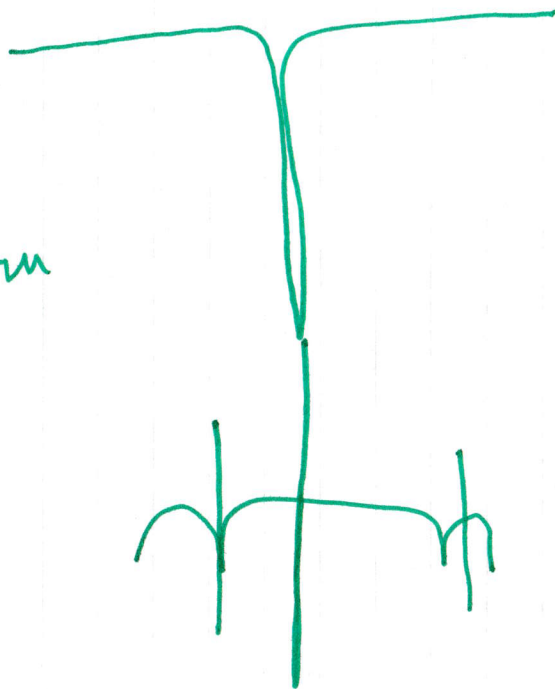
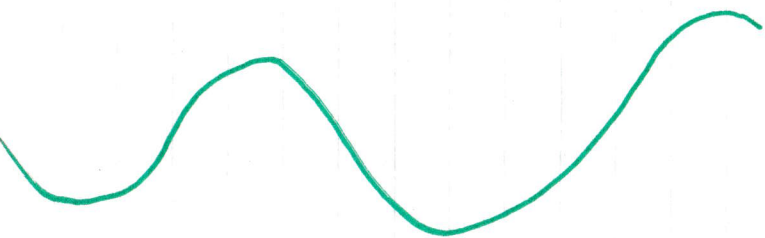
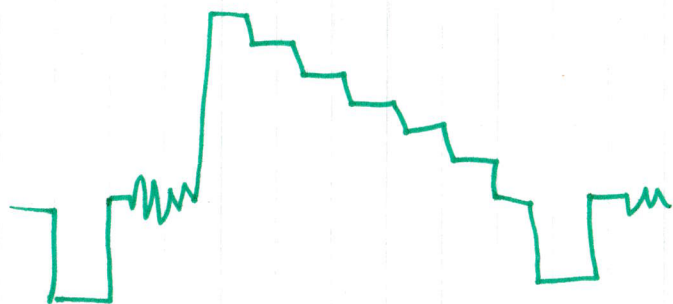
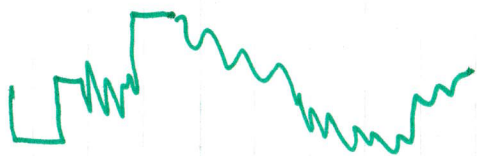


1 of 4 Board types

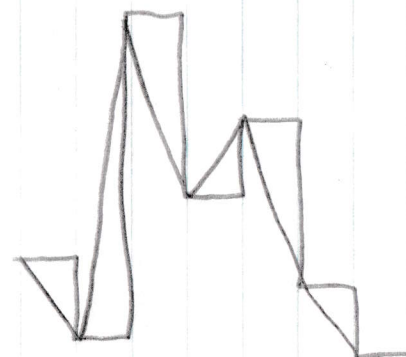
42











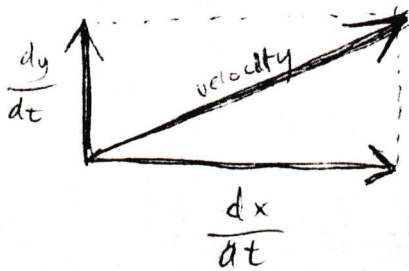


# INTENSITY COMPENSATION

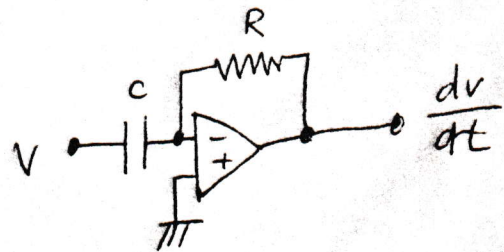
$$\sqrt{\frac{dx}{dt} + \frac{dy}{dt}} = \text{absolute velocity}$$

$$\frac{dx}{dt} = \text{horizontal velocity}$$

$$\frac{dy}{dt} = \text{vertical velocity}$$



$$\text{velocity} = \sqrt{\left(\frac{dy}{dt}\right)^2 + \left(\frac{dx}{dt}\right)^2}$$

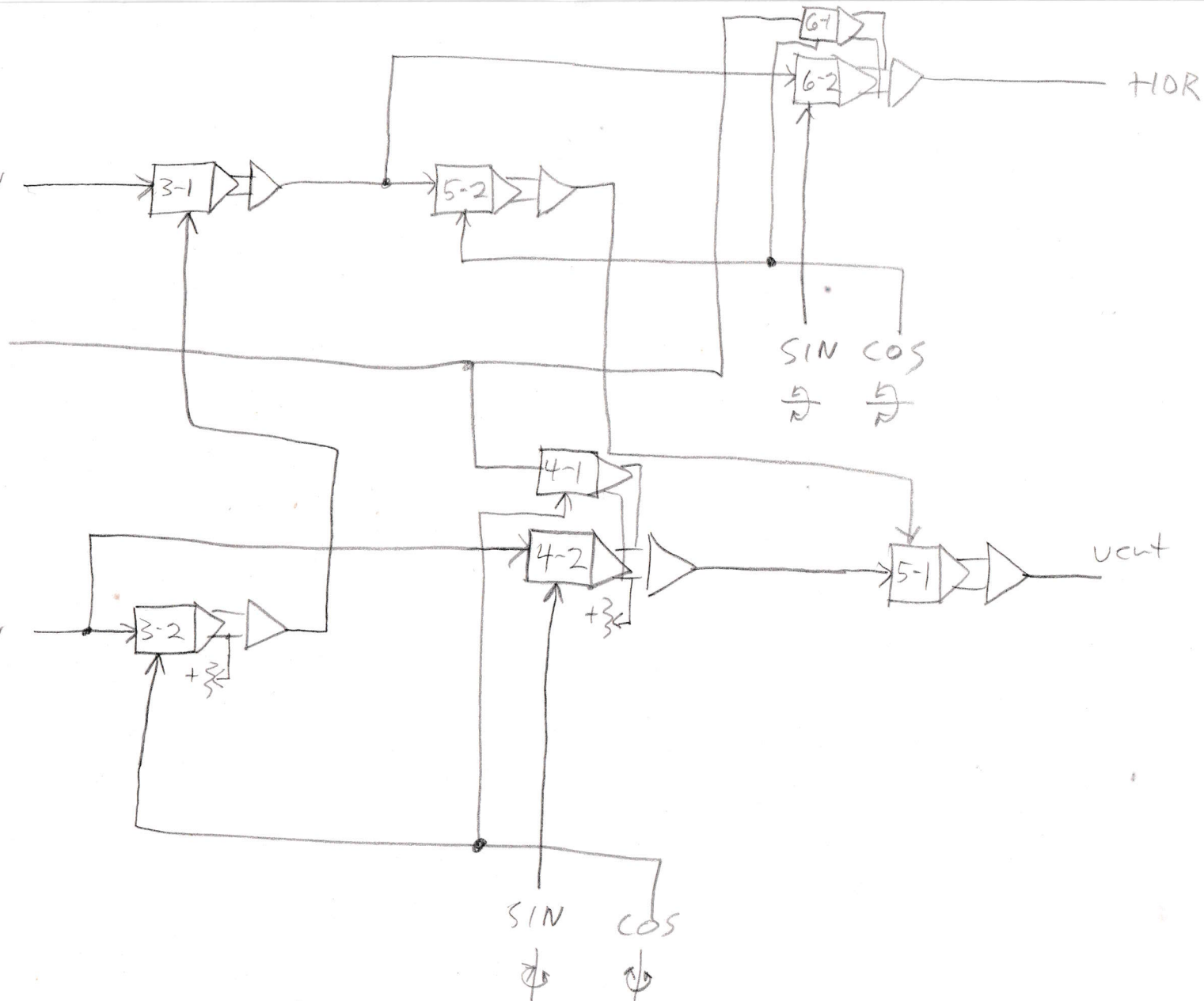




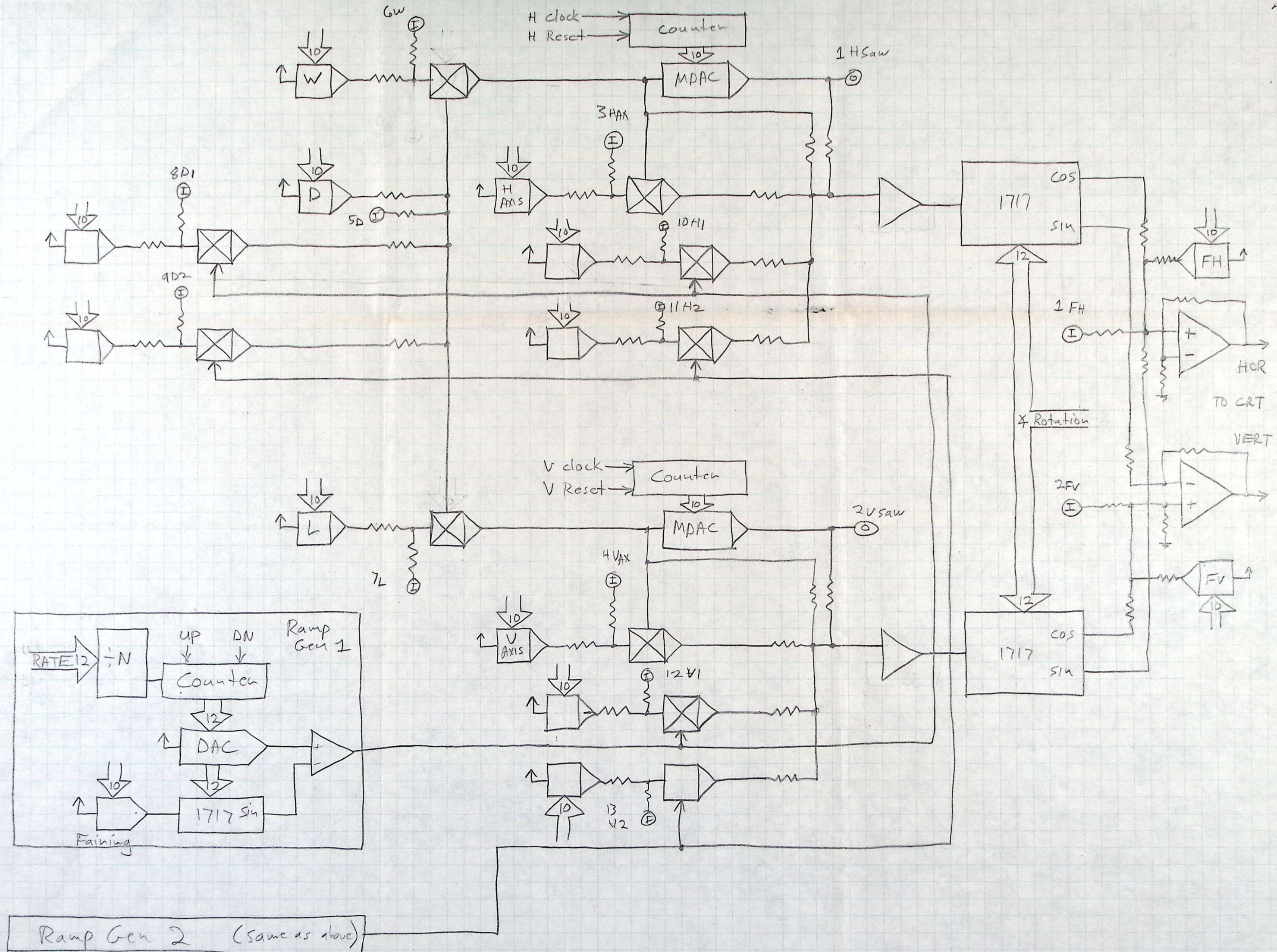
H Saw

VID

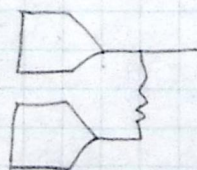
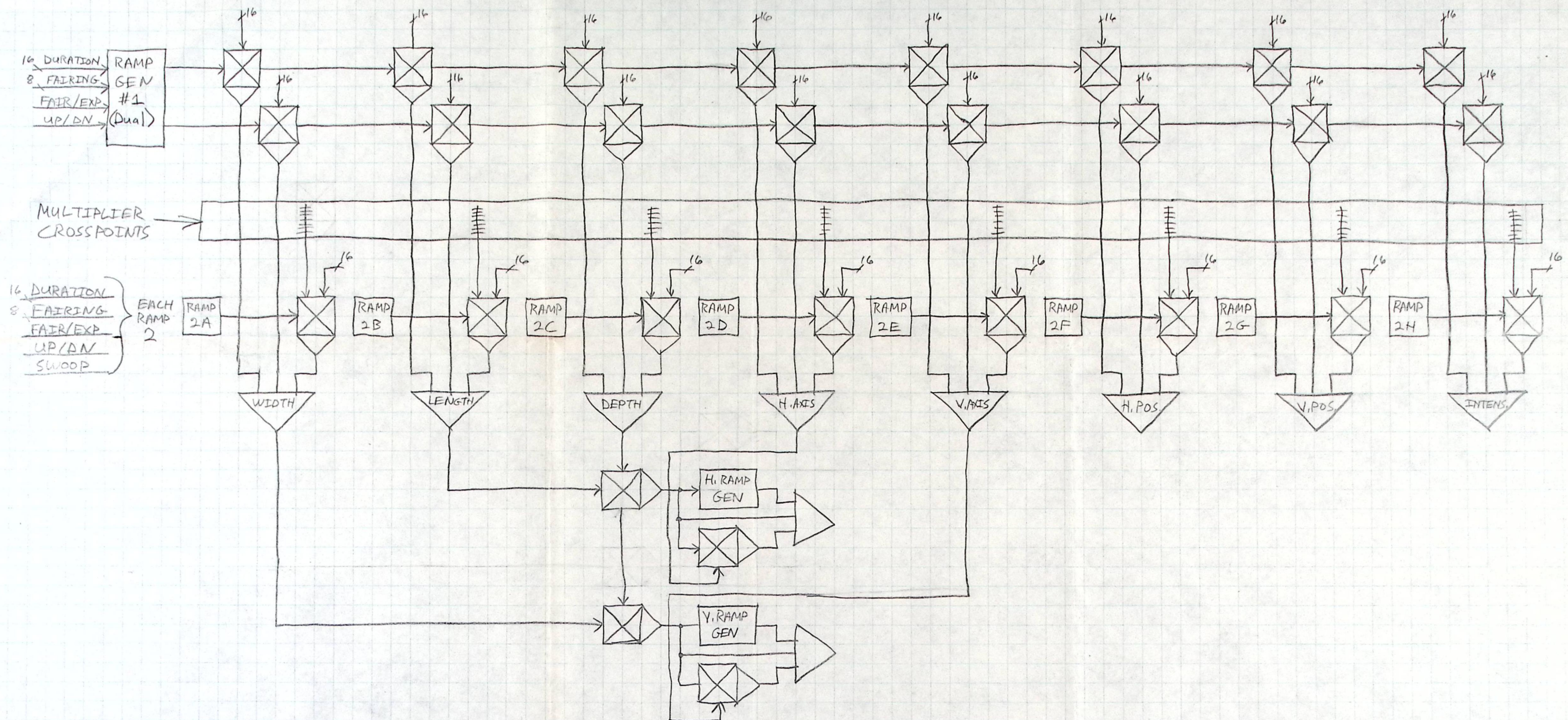
V Saw



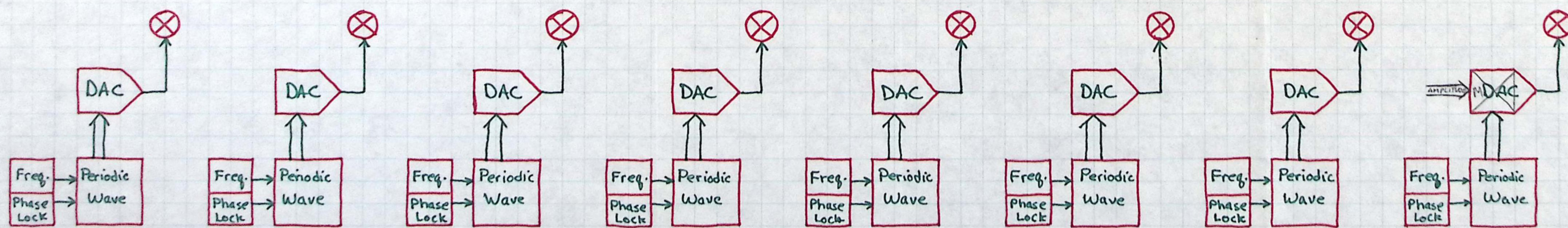
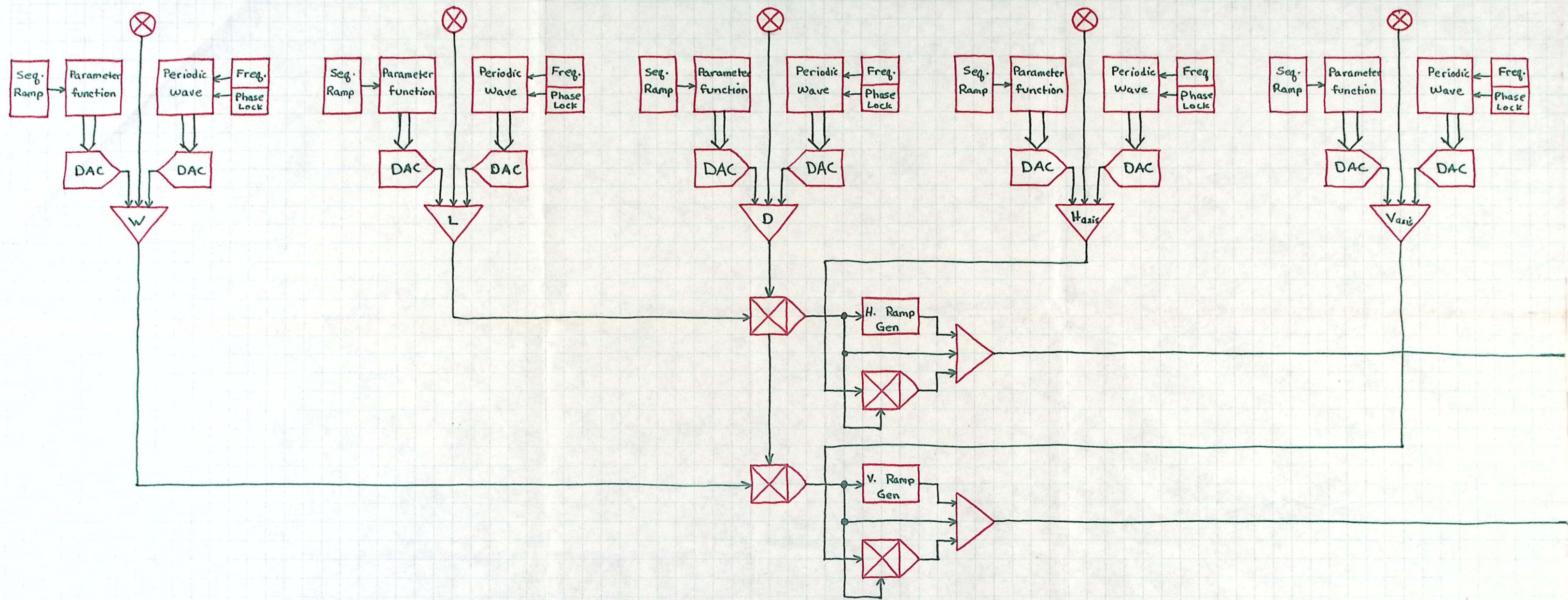




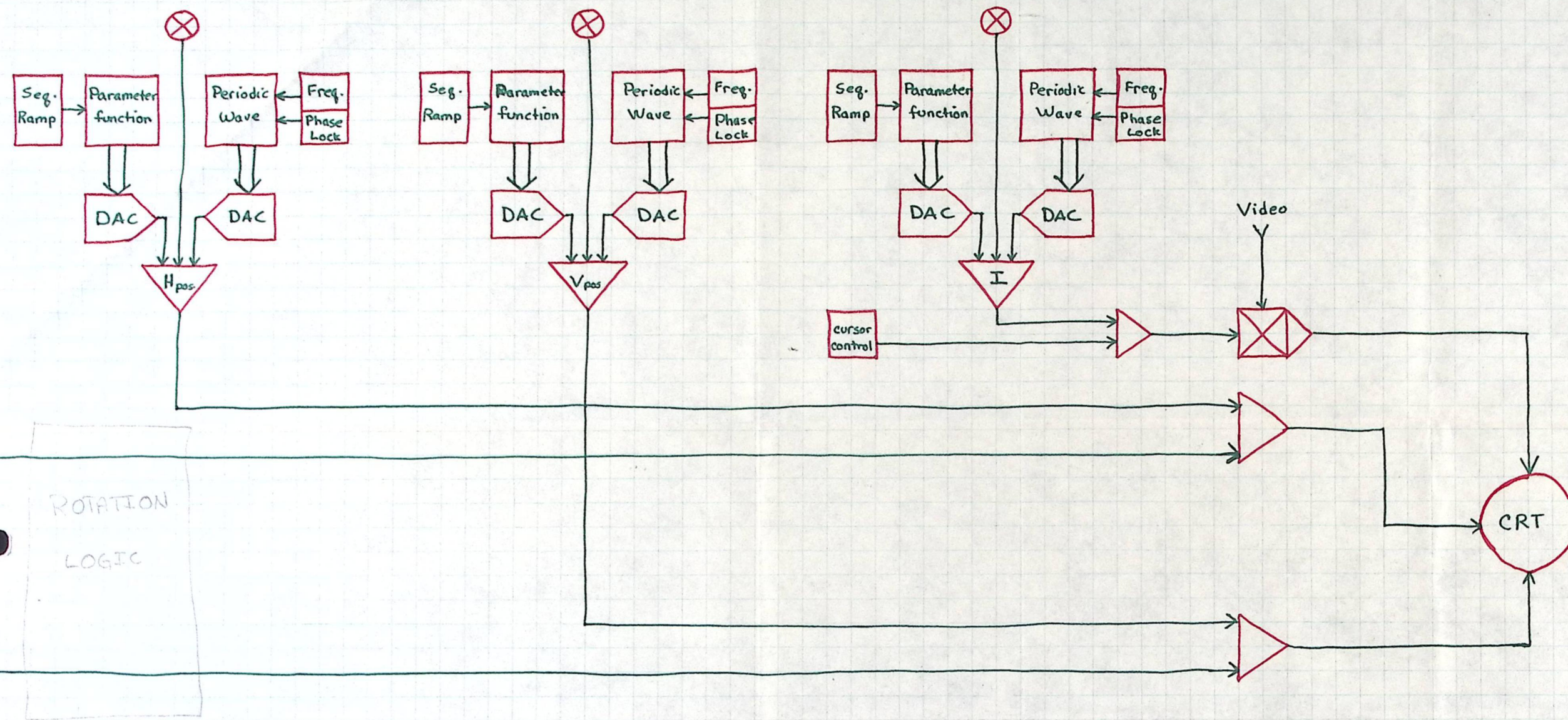




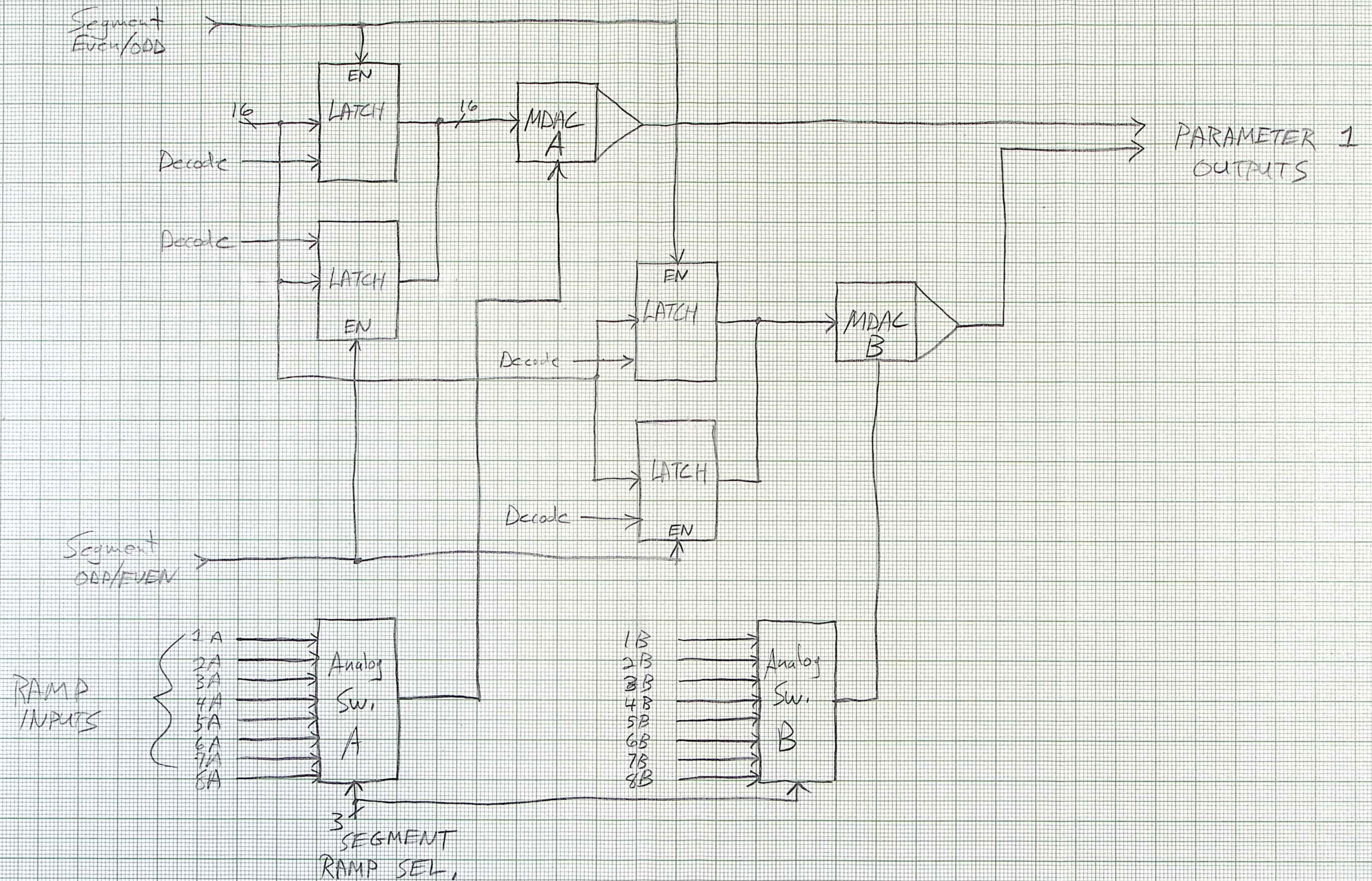




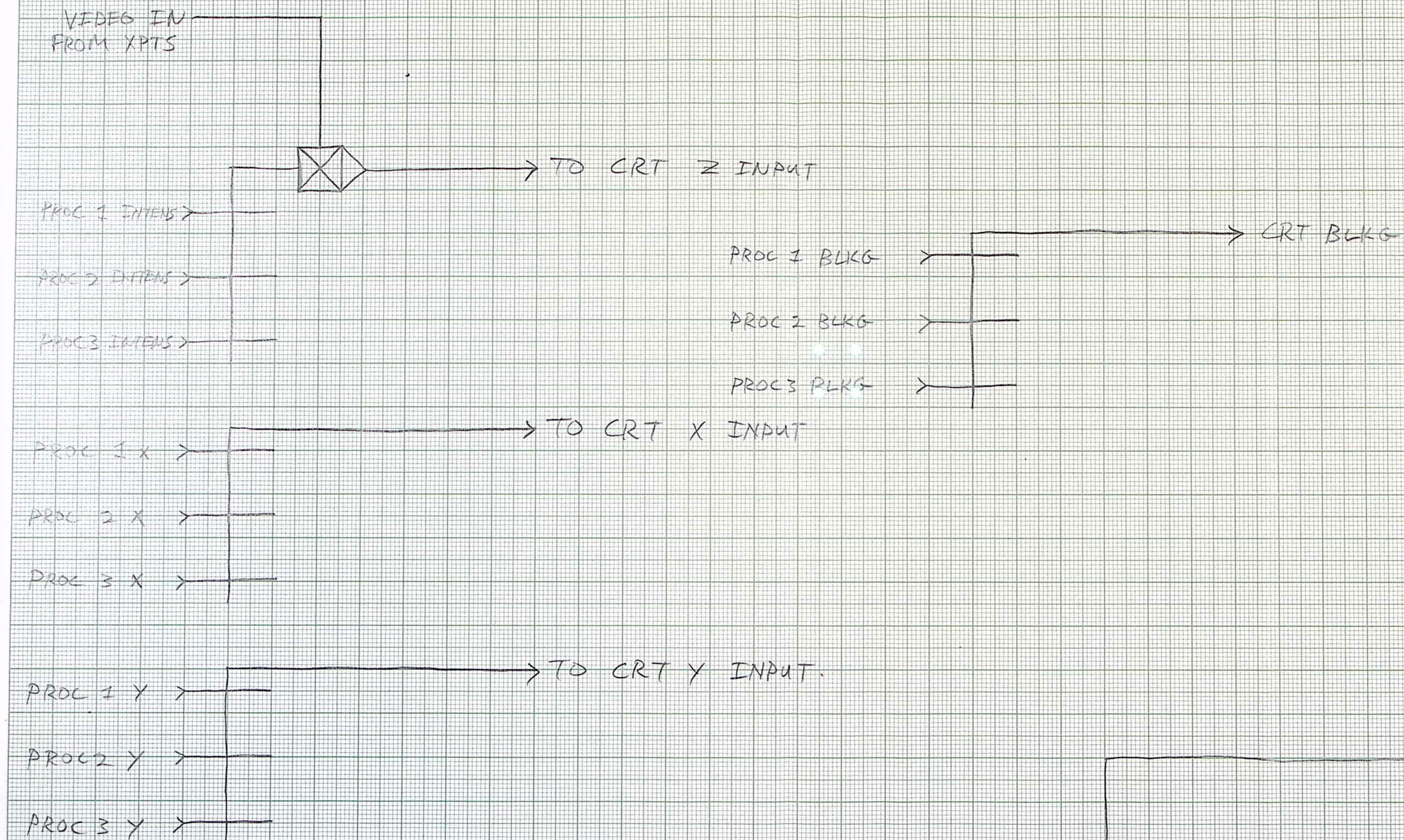




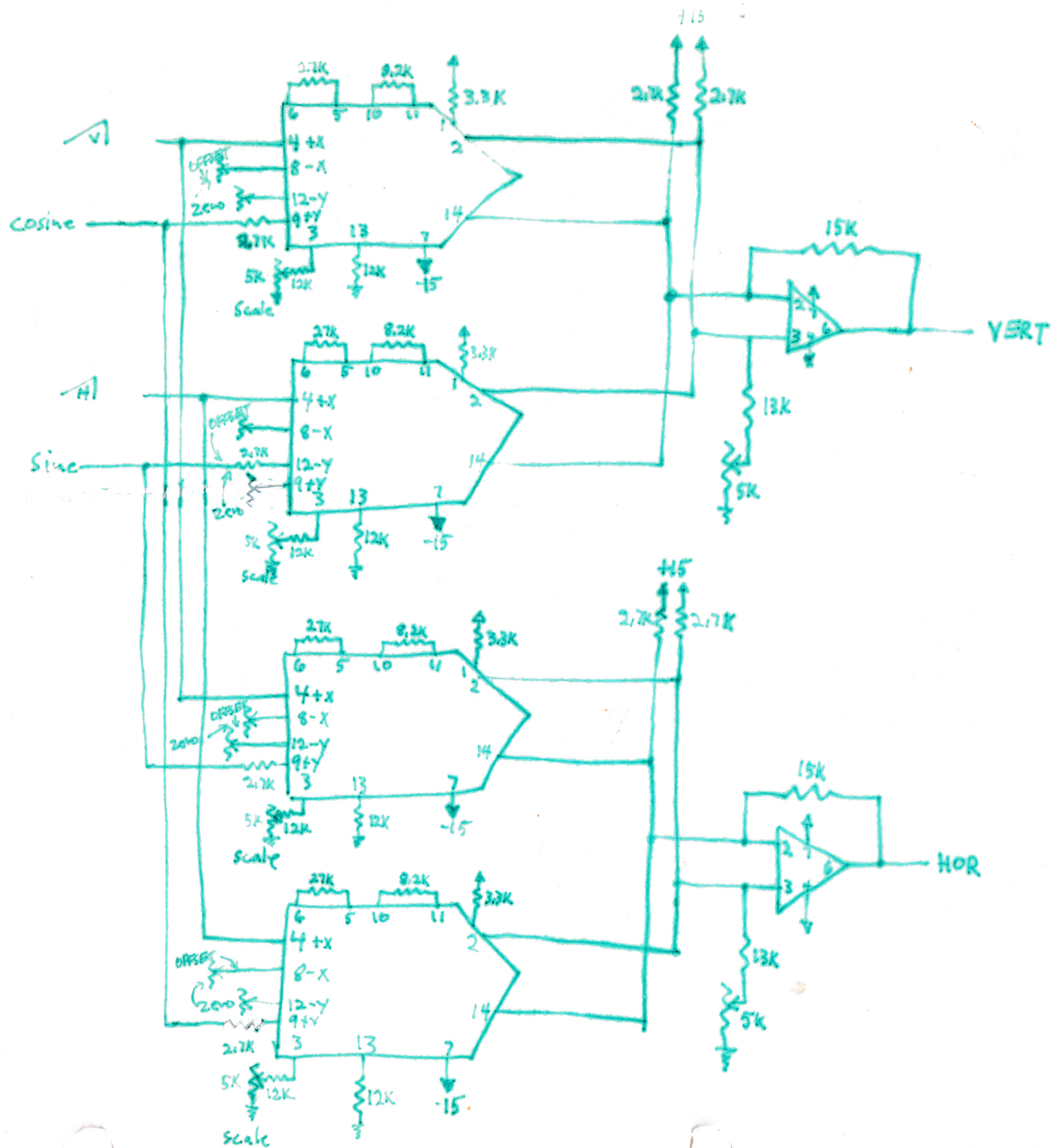












Very First Rotation  
Block 11-80



YAW (about x axis)

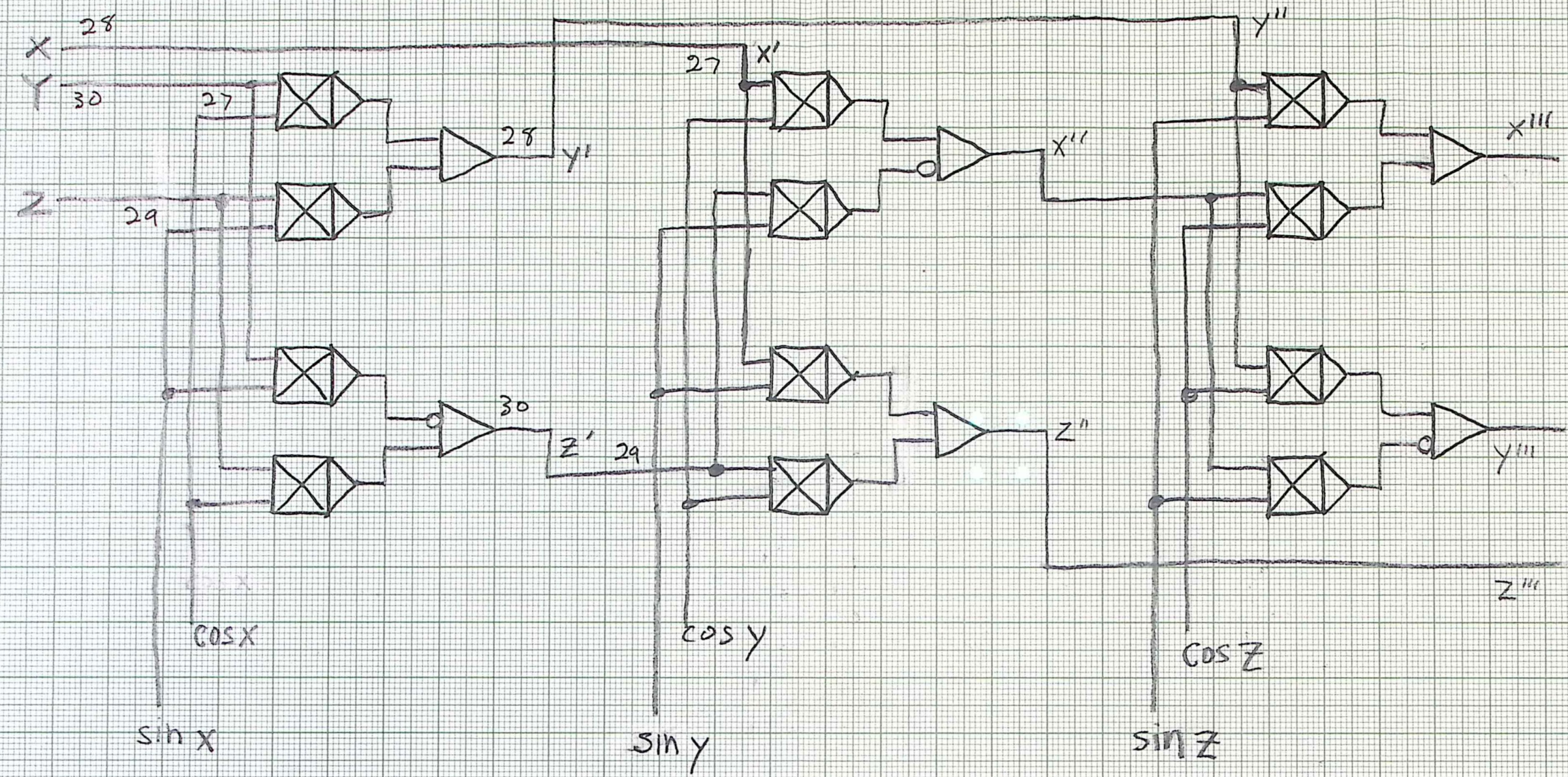
PITCH (about y axis)

ROLL (about z axis)

$$\begin{aligned} x' &= x \\ y' &= y \cos X + z \sin X \\ z' &= z \cos X - y \sin X \end{aligned}$$

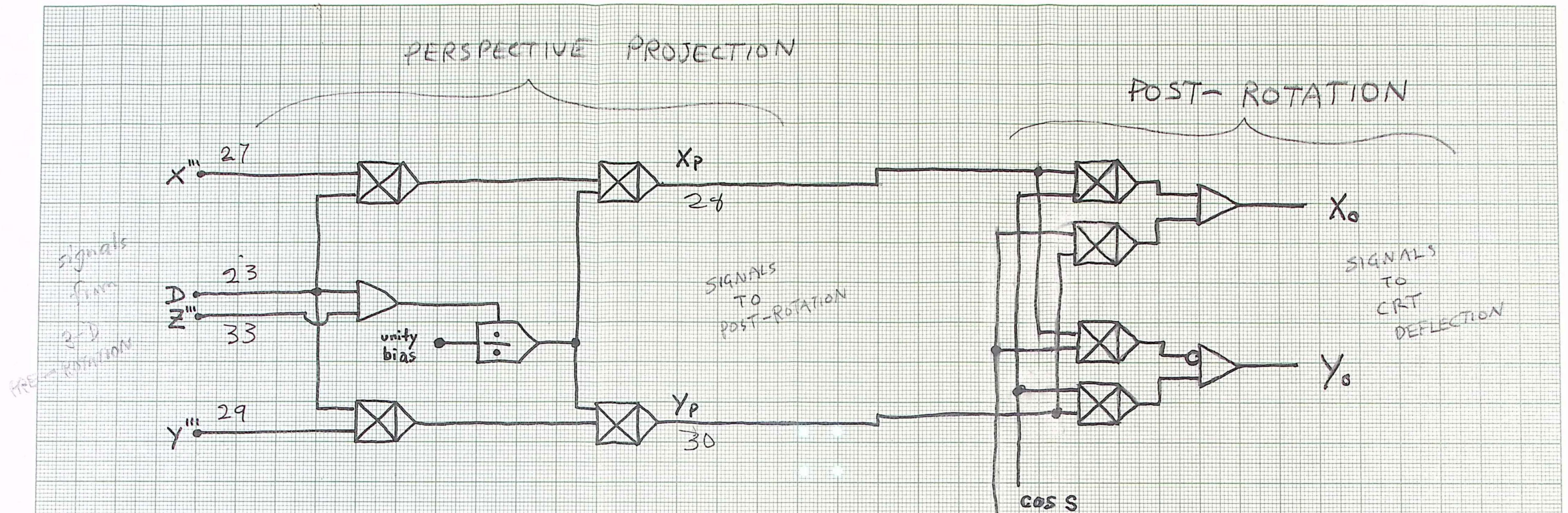
$$\begin{aligned} x'' &= x' \cos y - z' \sin y \\ y'' &= y' \\ z'' &= x' \sin y + z' \cos y \end{aligned}$$

$$\begin{aligned} x''' &= x'' \cos Z + y'' \sin Z \\ y''' &= y'' \cos Z - x'' \sin Z \\ z''' &= z'' \end{aligned}$$



signals  
to perspective  
projection





unity bias = arbitrary positive voltage (bias for unity gain)

D = zoom (focal length of simulated lens)

Z''' = DEPTH

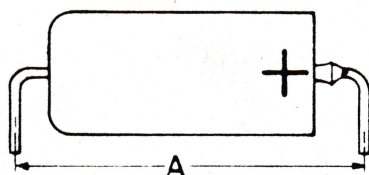
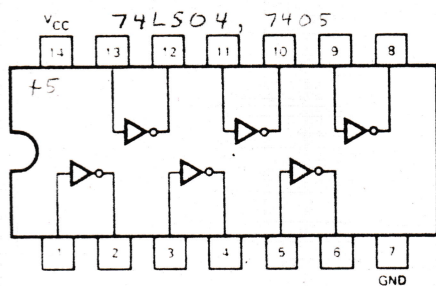
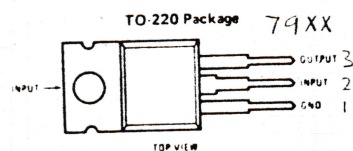
$$X_p = \frac{X''' D}{Z''' + D} = (X''' D) \frac{1}{Z''' + D} = \frac{X'''}{(Z'''/D) + 1}$$

$$Y_p = \frac{Y''' D}{Z''' + D} = (Y''' D) \frac{1}{Z''' + D} = \frac{Y'''}{(Z'''/D) + 1}$$

$$X_0 = X_p \cos S + Y_p \sin S$$

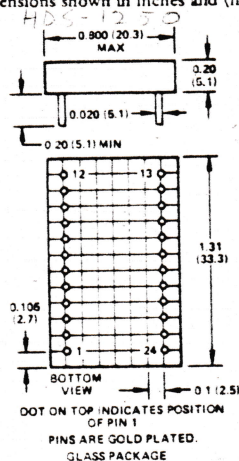
$$Y_0 = Y_p \cos S - X_p \sin S$$



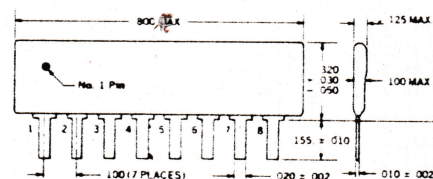
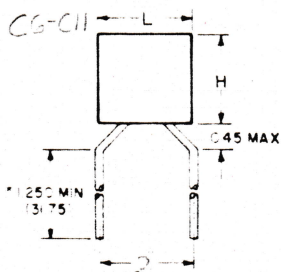
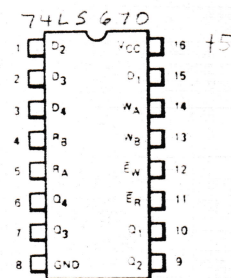
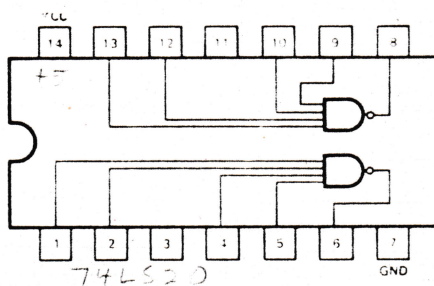
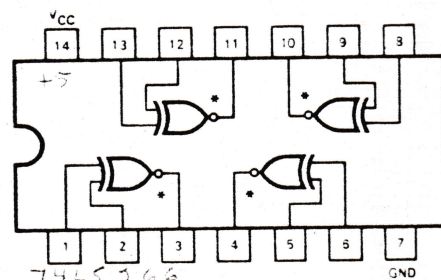
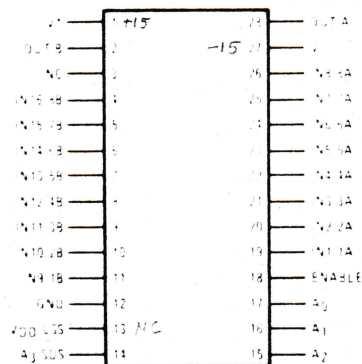
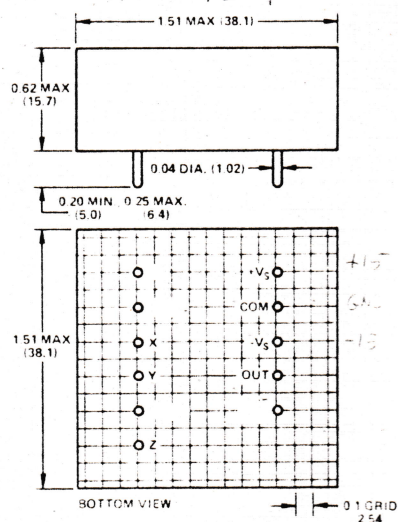


C1-3 = 1.1"  
C4-5 = 0.5"

PIN	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12
13-19	GND
20	OUTPUT
21	R <sub>L</sub> 200Ω
22	BIPOLAR OFFSET
23	-15V
24	+15V



AD-429





# BOARD #'S

AS-100-A	-	Interface Board
AS-200-A	-	Card Cage Motherboard
AS-300-A	-	Bus Buffer
AS-310-A	-	Raster Gen
AS-320-A	-	Rotation
AS-330-A	-	Depth
AS-340-A	-	CRT DRVR
AS-350-A	-	BLKG
AS-360-A	-	PMT Video
AS-370-A	-	INT. COMP
AS-380-A	-	SEG. PRIO.
AS-390-A	-	SEG STATUS
AS-400-A	-	PARA. CONT.
AS-410-A	-	Analog I'face
AS-500-A	-	PMT PreAmp

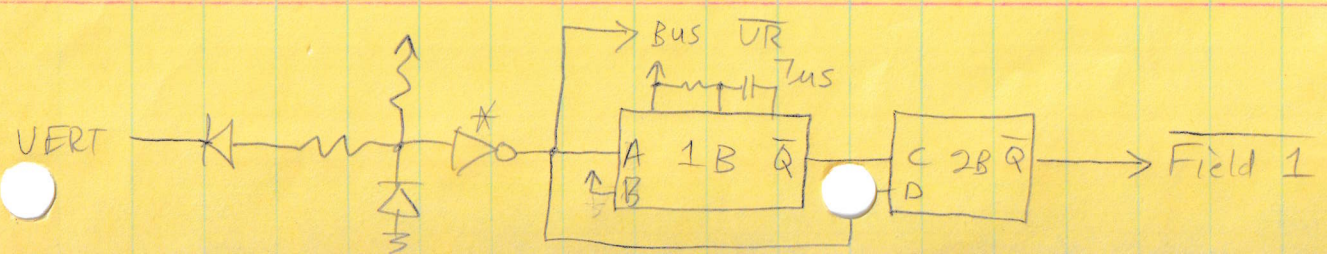
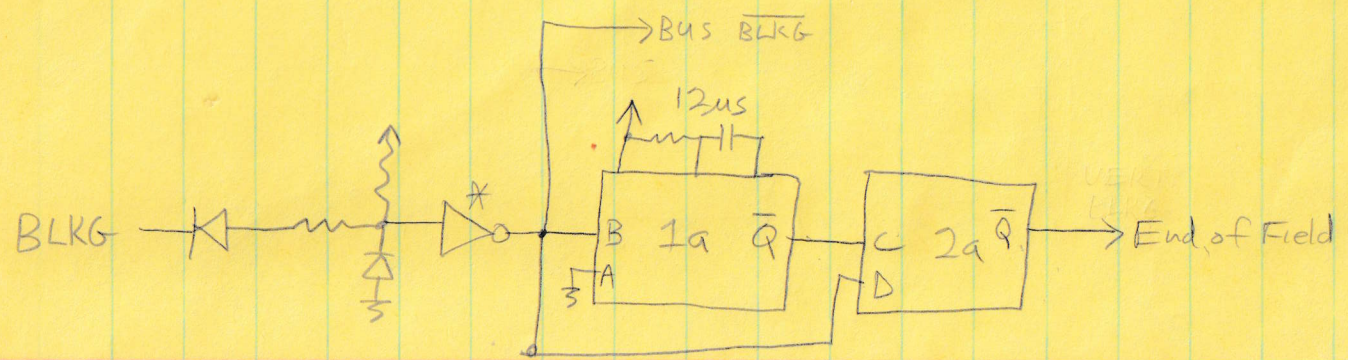
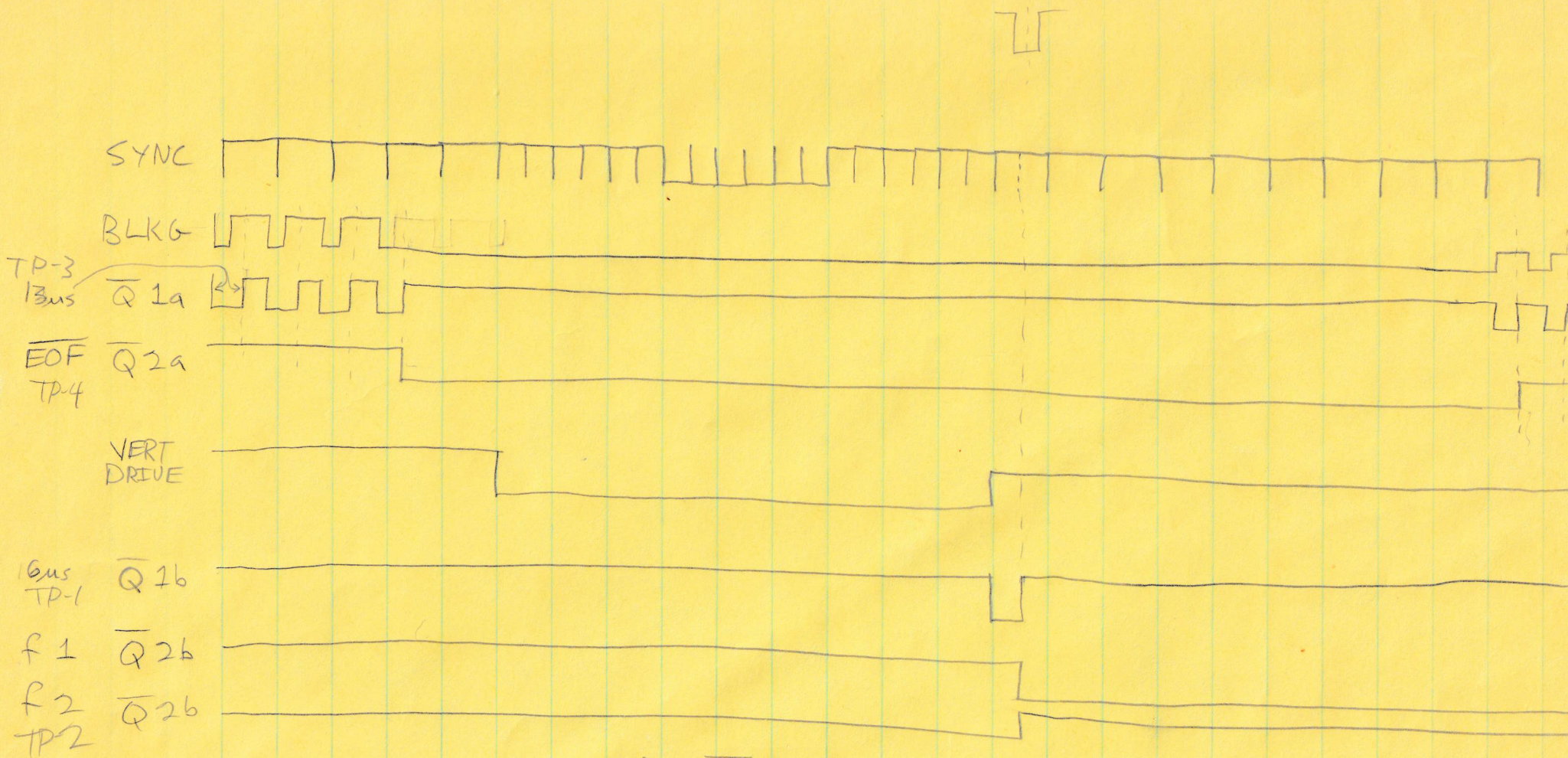
CHUCK  
SLEZAK



# Prototype Bus

Card	Function	#Addresses	Base Address	DIPsw M L
A.	Bus Buffer	8		
B.	Raster + Axis	8		
C.	X Rotation	8	0000	0000
D.	Y Rotation	8	0020	0001
E.	Z Rotation	8	0040	0010
F.	Post Rotation	8	0060	0011
G.	Depth + Relief	8		
H.	CRT Driver	8		
J.	Xsize Parameter	24	0200	0000
K.	Xsize "	24	0220	0001
L.	X AXIS " 2500	24	0240	0010
M.	Y AXIS " 3500	24	0260	0011
N.	Depth "	24	0280	0100
FOCAL P.	<del>Relief</del> " 4095	24	02A0	0101
R.	X pos "	24	02C0	0110
S.	Y pos "	24	02E0	0111
T.	Red Video	16	0400	0000
V.	Green Video	16	0420	0001
W.	Blue Video	16	0440	0010
X.	Intensity Comp	—	✓	
Y.	Segment Control	8	0600	0000







## CU-3 outputs

0 EW 1A } FU1, P1 BIAS  
 1 EW 2A }  
 2 EW 1B } FU2, P1 AMP  
 3 EW 2B }  
 4 EW 3A } JU1+5 P1 EXT  
 5 EW 4A }  
 6 EW T1  
 7 EW S (NORM/HIRES)

## CU 4 outputs

0 EW 1C } FU3, P2 BIAS  
 1 EW 2C }  
 2 EW 1D } FU4, P2 AMP  
 3 EW 2D }  
 4 EW 3B } JU2,6 P2 EXT  
 5 EW 4B }  
 6 EW T2

## CU-5 outputs

0 EW 1E } FU5 P3 BIAS  
 1 EW 2E }  
 2 EW 1F } FU6 P3 AMP  
 3 EW 2F }  
 4 EW 3C } JU3,7 P3 EXT  
 5 EW 4C }  
 6 EW T3  
 7

## CU-6

0 EW 1G } FU7, P4 BIAS  
 1 EW 2G }  
 2 EW 1H } FU8, P4 AMP  
 3 EW 2H }  
 4 EW 3D } JU4,8 P4 EXT  
 5 EW 4D }  
 6 EW T4  
 7



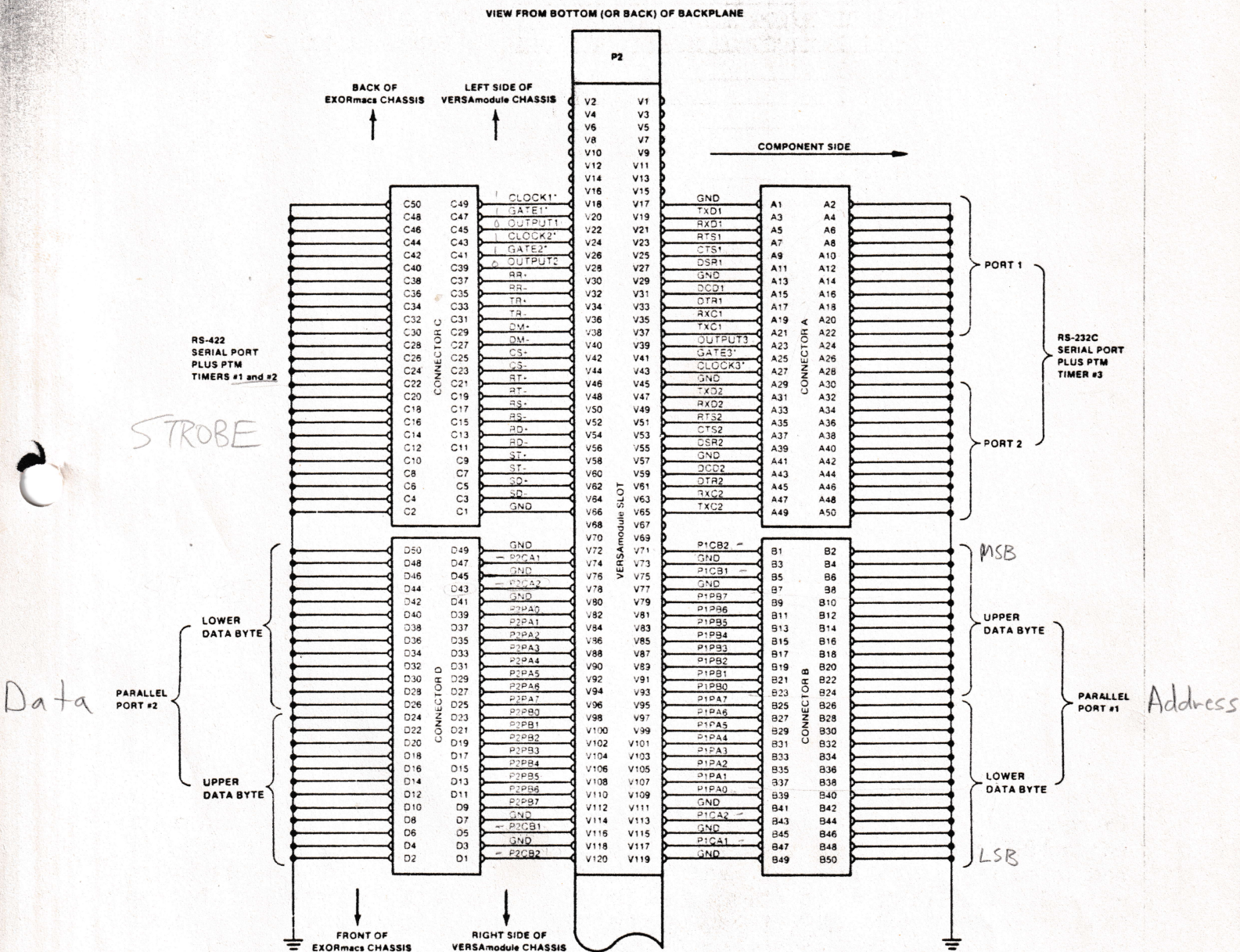
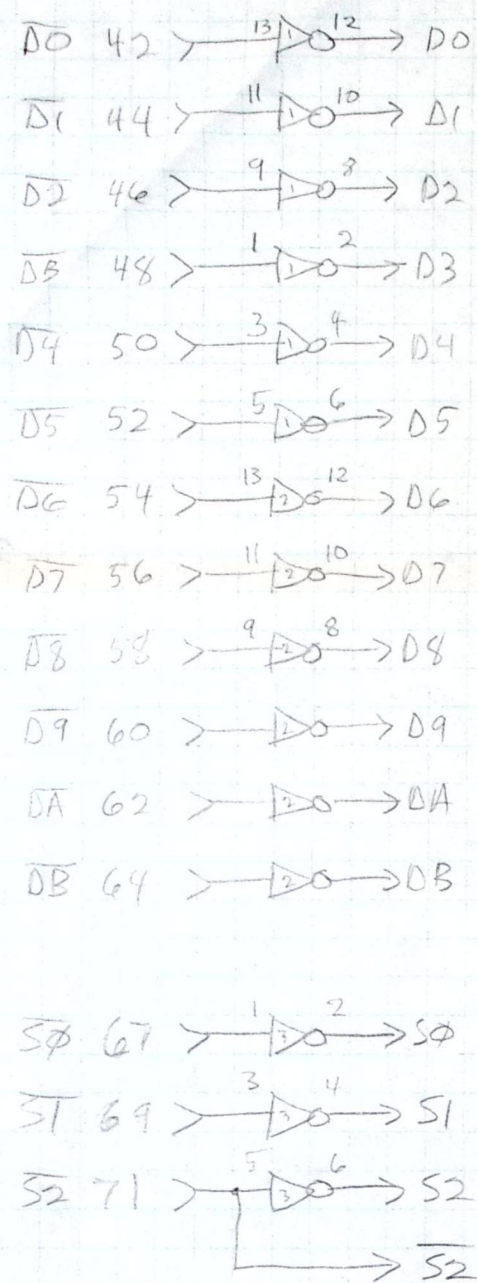


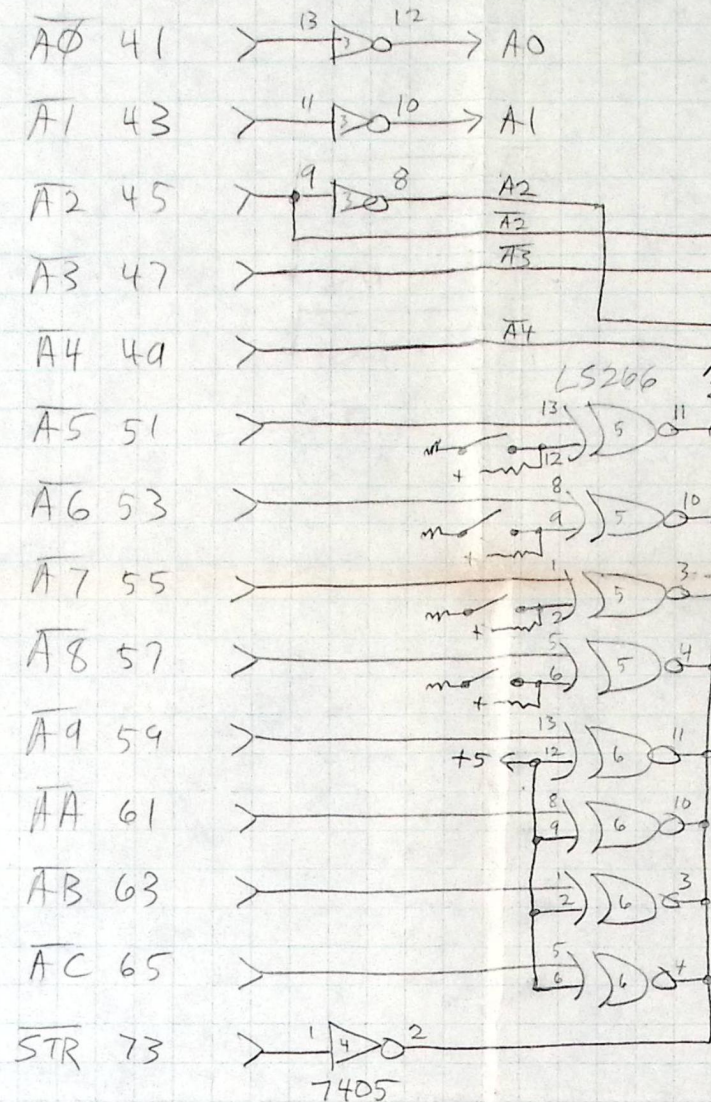
FIGURE 2-21. Peripheral Cable Connections to EXORmacs Chassis or to VERSAmodule Chassis (Sheet 1 of 2)



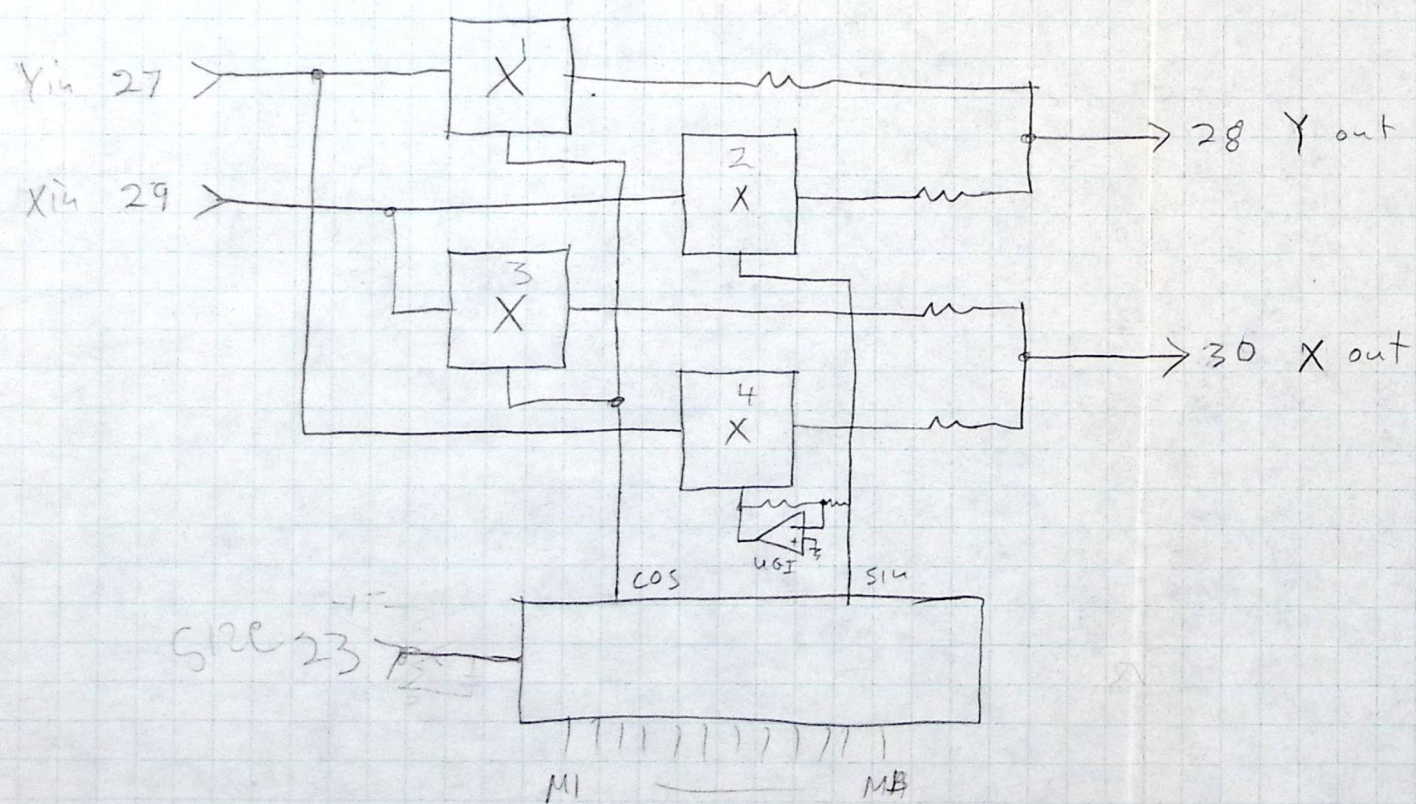
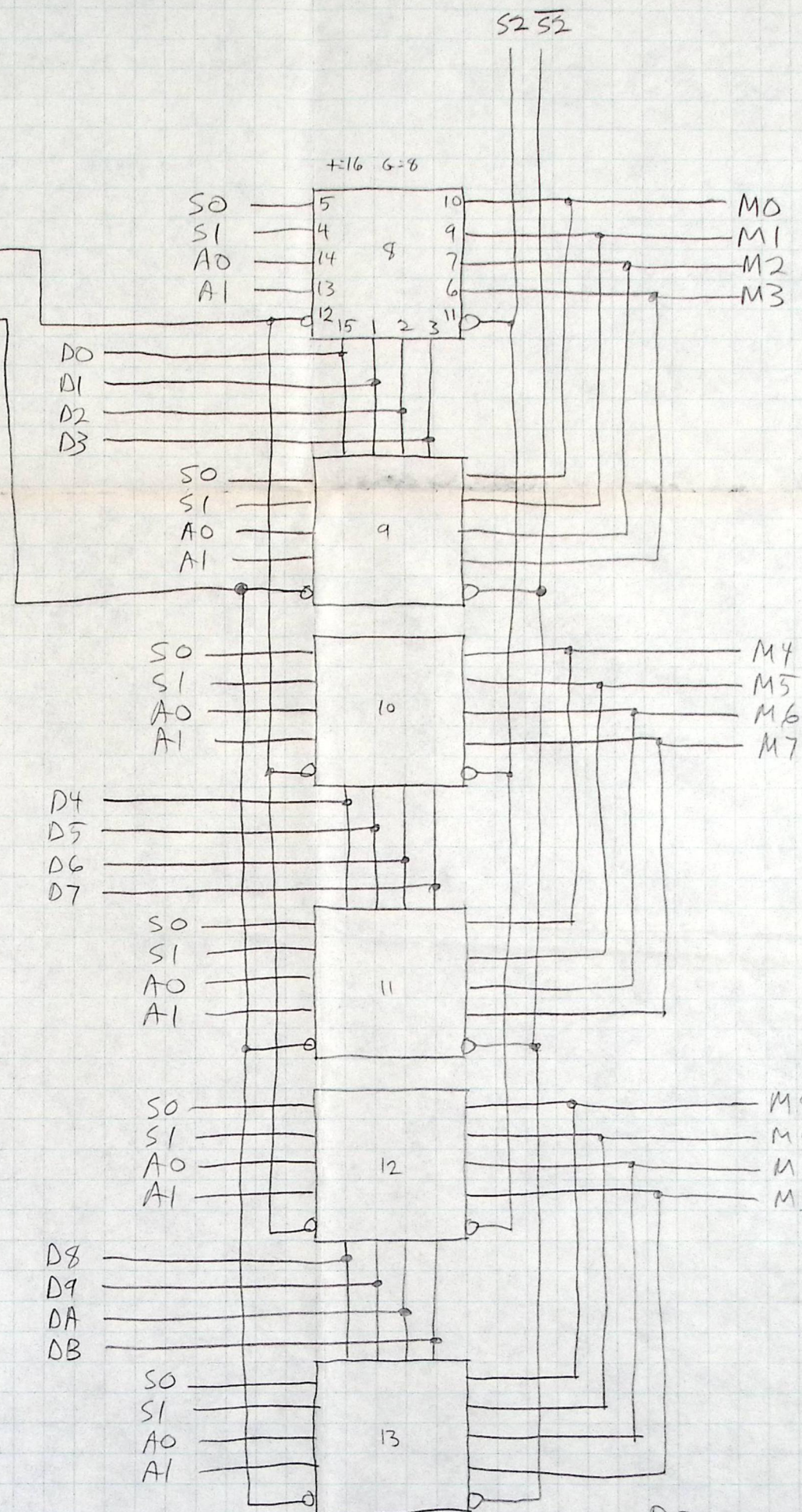
LS04



LS04



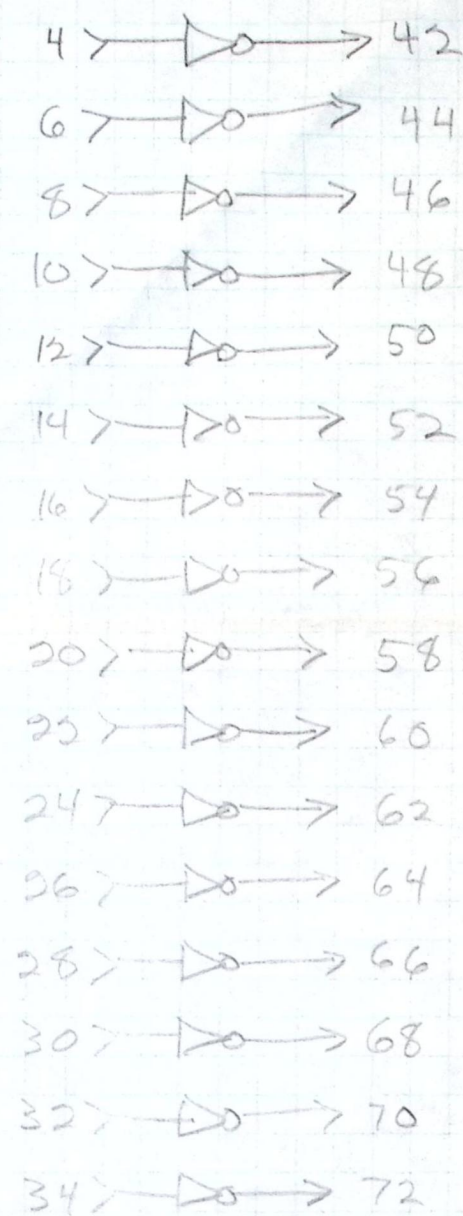
LS20



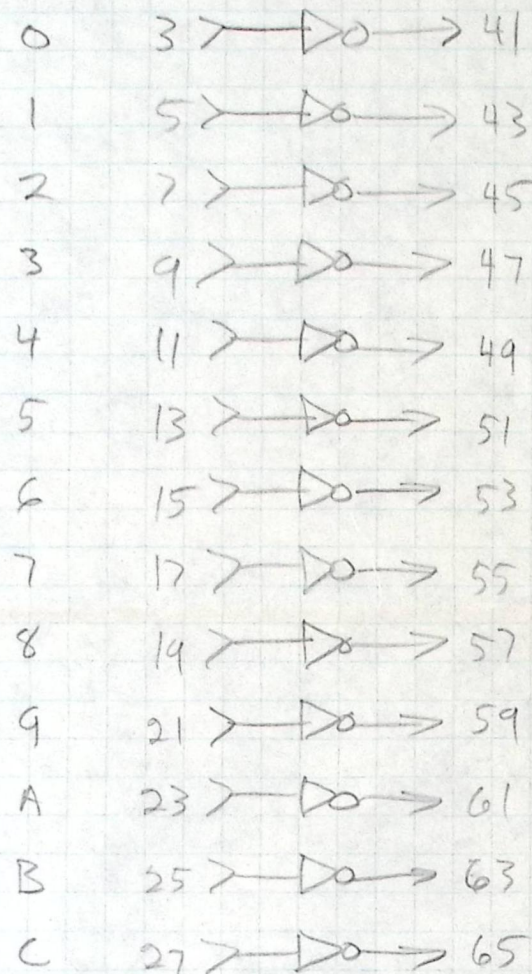
PROTOTYPE  
 Rotation Card  
 4-15-81 DWS



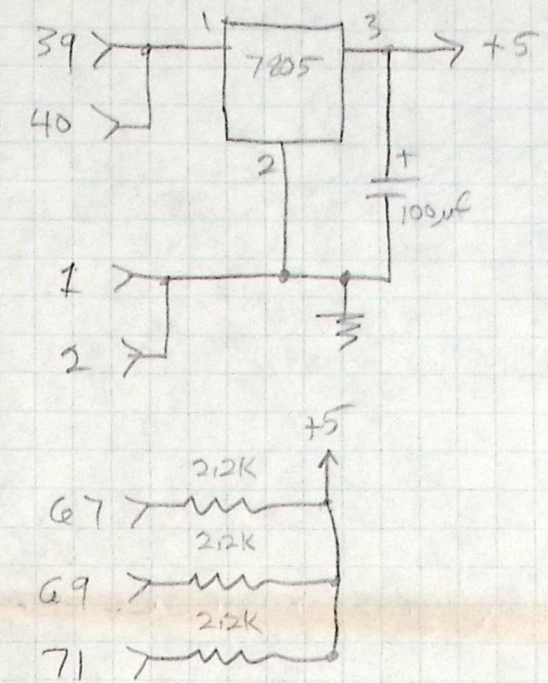
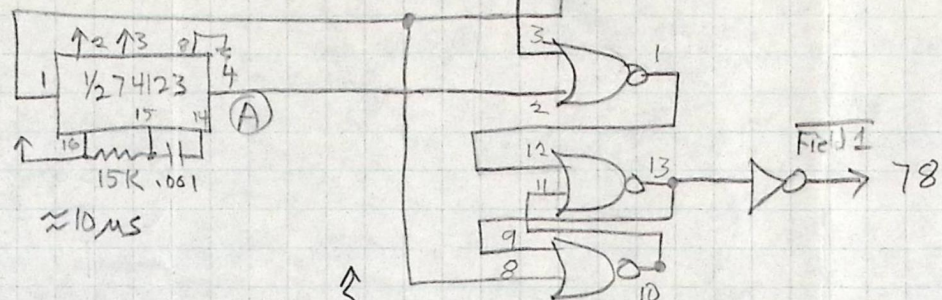
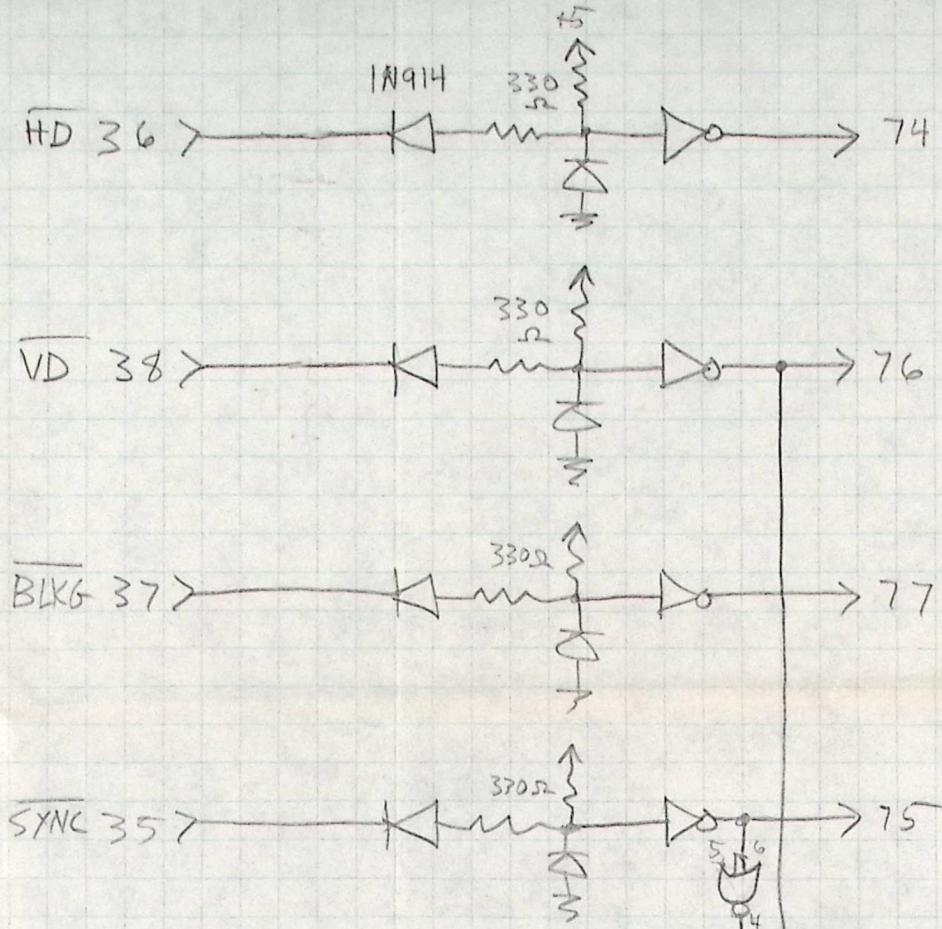
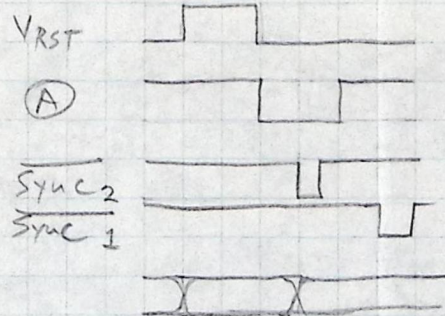
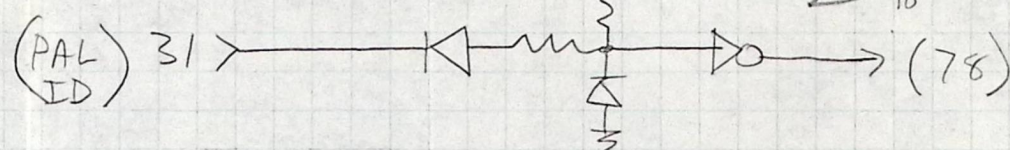
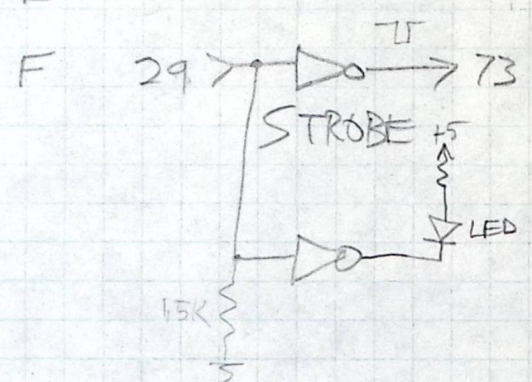
7405



DATA

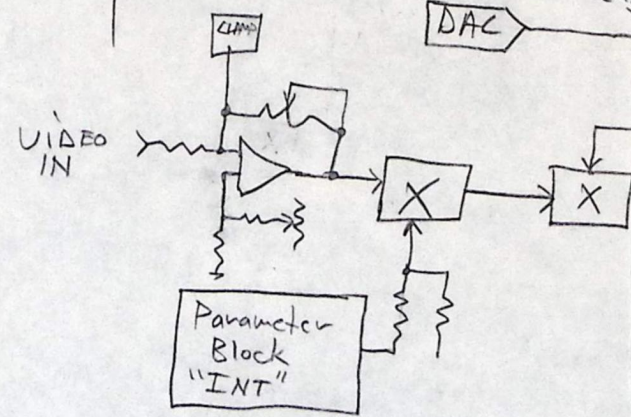
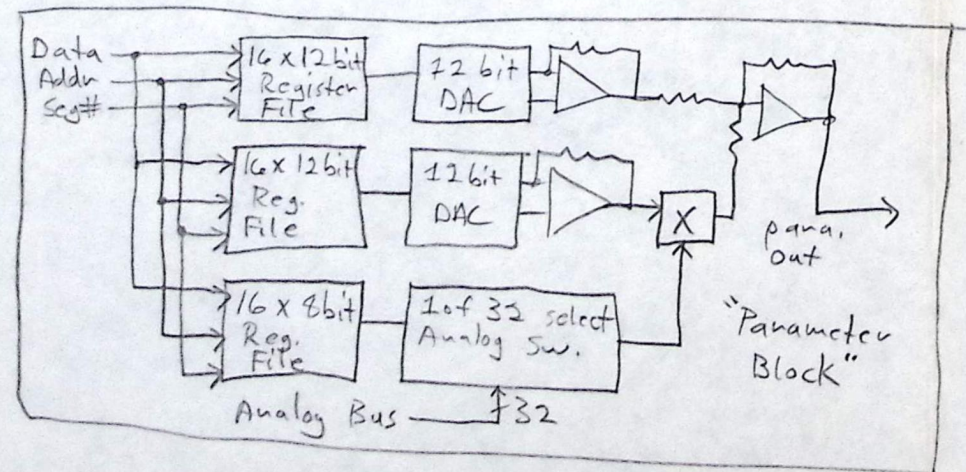
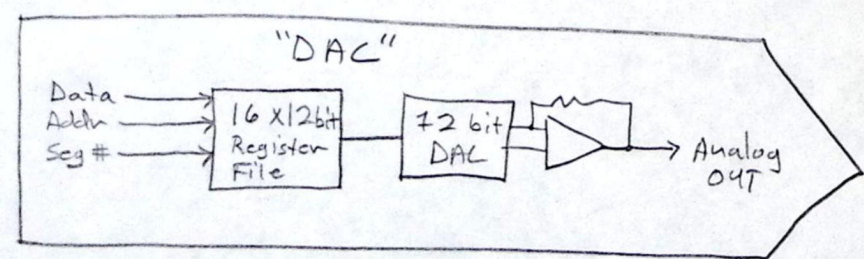
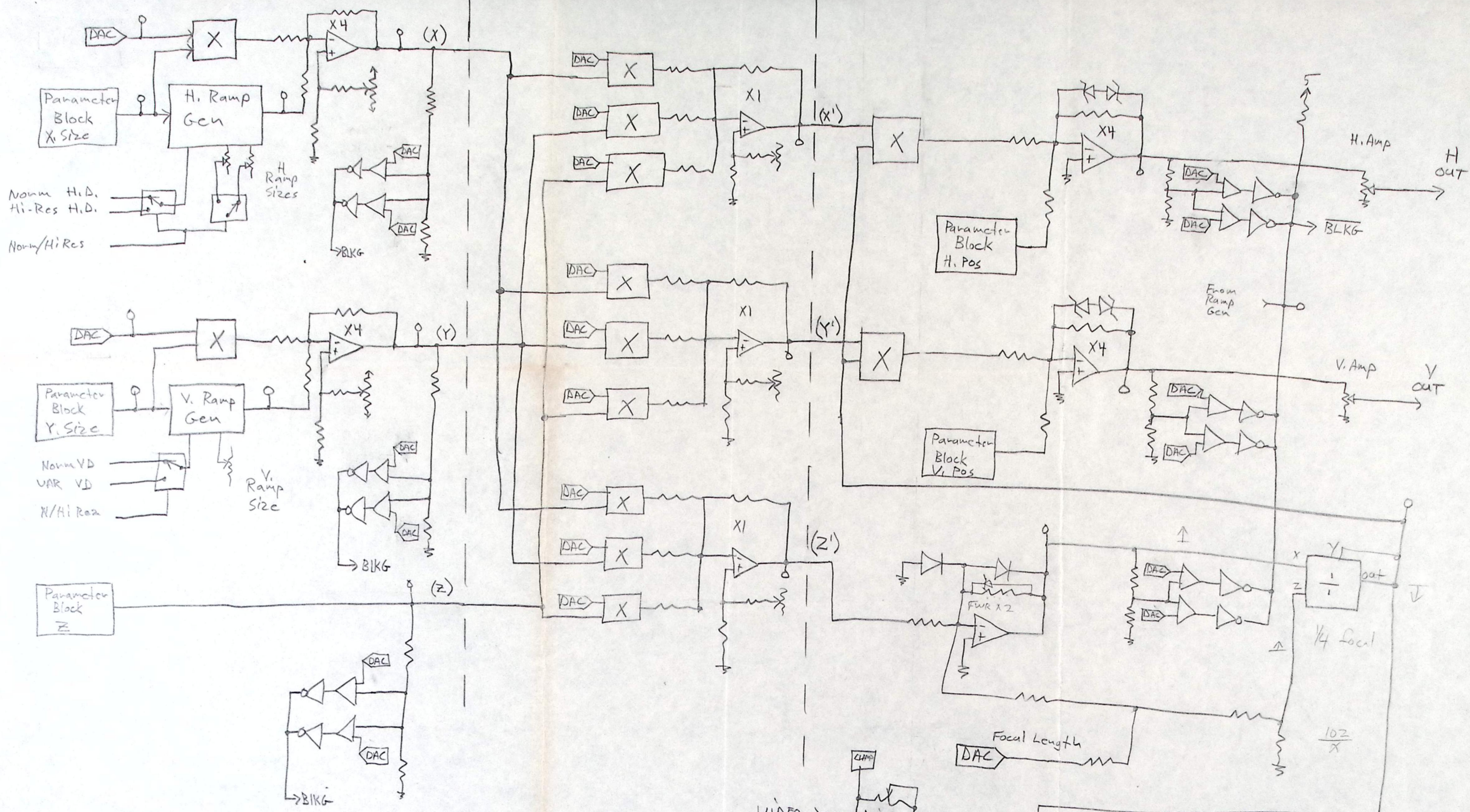


Address



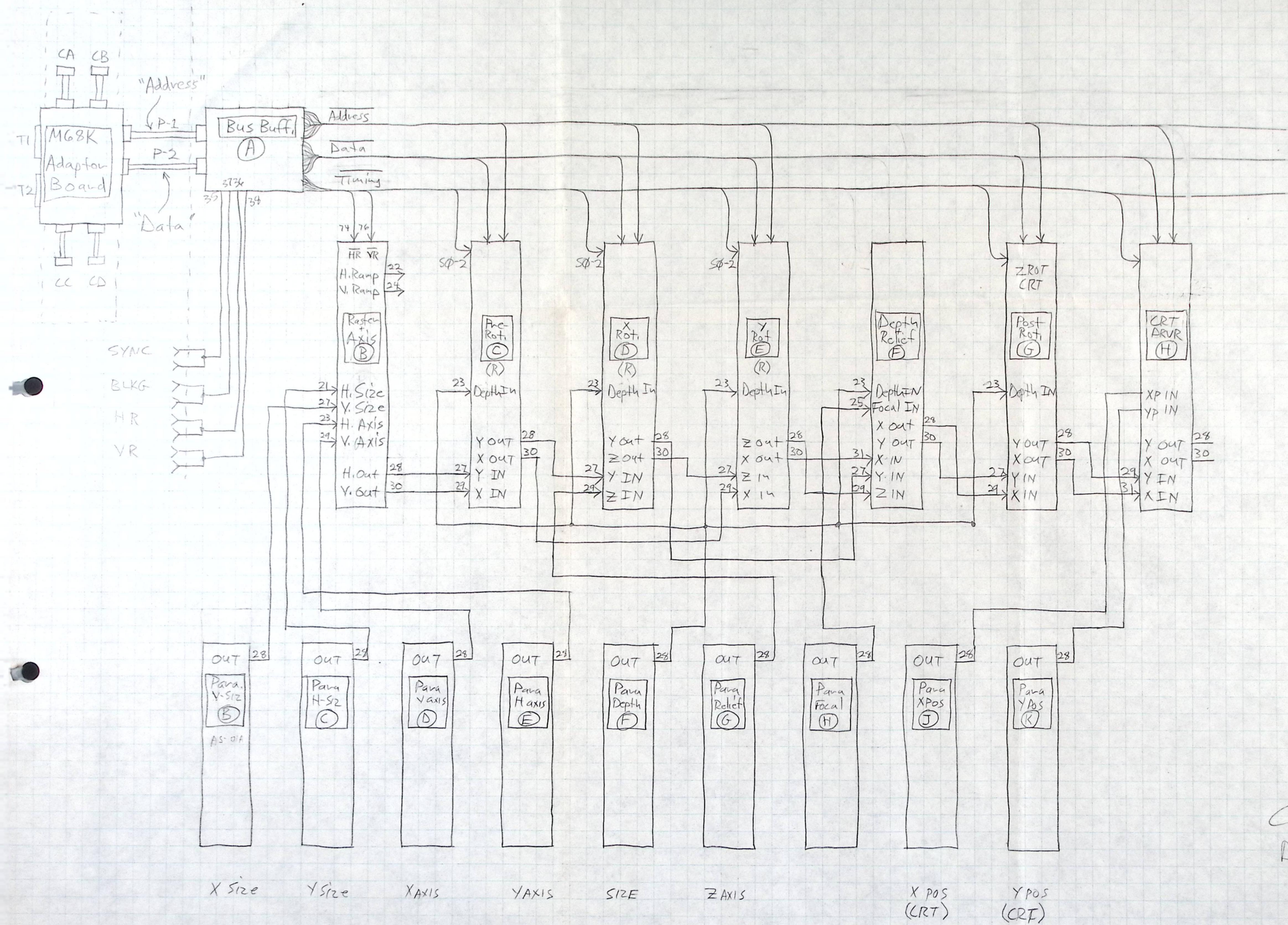
PROTOTYPE  
Bus Buffer Card "A"  
4-1-81 DWS





TEST SYSTEM BLOCK  
5/7/81







76 X 90 holes, 1"

# 3673 Proto Board Pinouts Wiring Side (Right)

1+2

① GROUND

④ Analog Bus 1

⑥ " 3

⑧ " 5

⑩ " 7

⑫ " 9

⑭ " B

⑯ " D

⑰ " F

⑲

⑳

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③ Analog Bus 0

⑤ " 2

⑦ " 4

⑨ " 6

⑪ " 8

⑬ " A

⑮ " C

⑰ " E

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Analog Bus except for Card # A (Digital and Sync) Inputs

OUTPUTS

INPUTS

+8V

+18V

④ DATA 0

⑥ " 1

⑧ " 2

⑩ " 3

⑫ " 4

⑭ " 5

⑯ " 6

⑰ " 7

⑱ " 8

⑲ " 9

㉑ " A

㉒ " B

㉓ " C

㉔ " D

㉕ " E

㉖ " F

㉗ H Reset

㉘ V Reset

㉙

㉚

㉛

④ ADDR. 0

⑥ " 1

⑧ " 2

⑩ " 3

⑫ " 4

⑭ " 5

⑯ " 6

⑰ " 7

⑱ " 8

㉑ " 9

㉒ " A

㉓ " B

㉔ " C

㉕ Seg. Addr. 0

㉖ " 1

㉗ " 2

㉘ STROBE

㉙ SYNC

㉚ BLKG

DIGITAL BUS SIGNALS

-18V

79+80

7VI

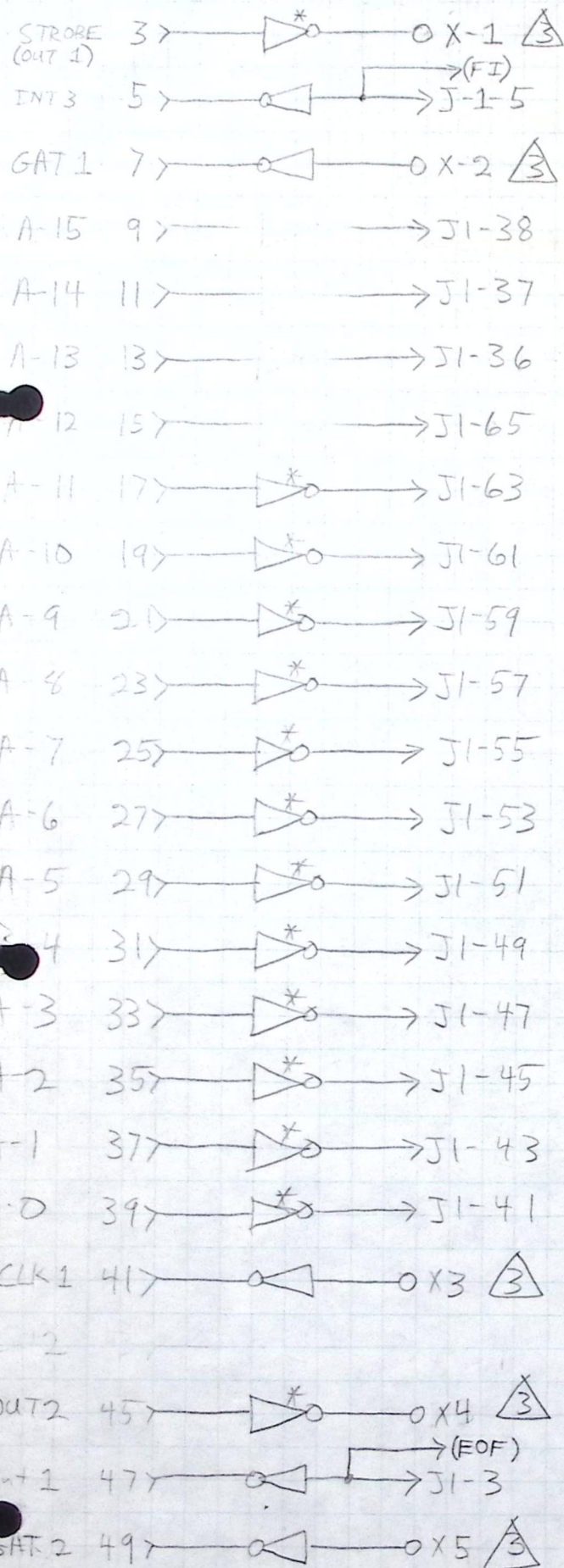
Field ID



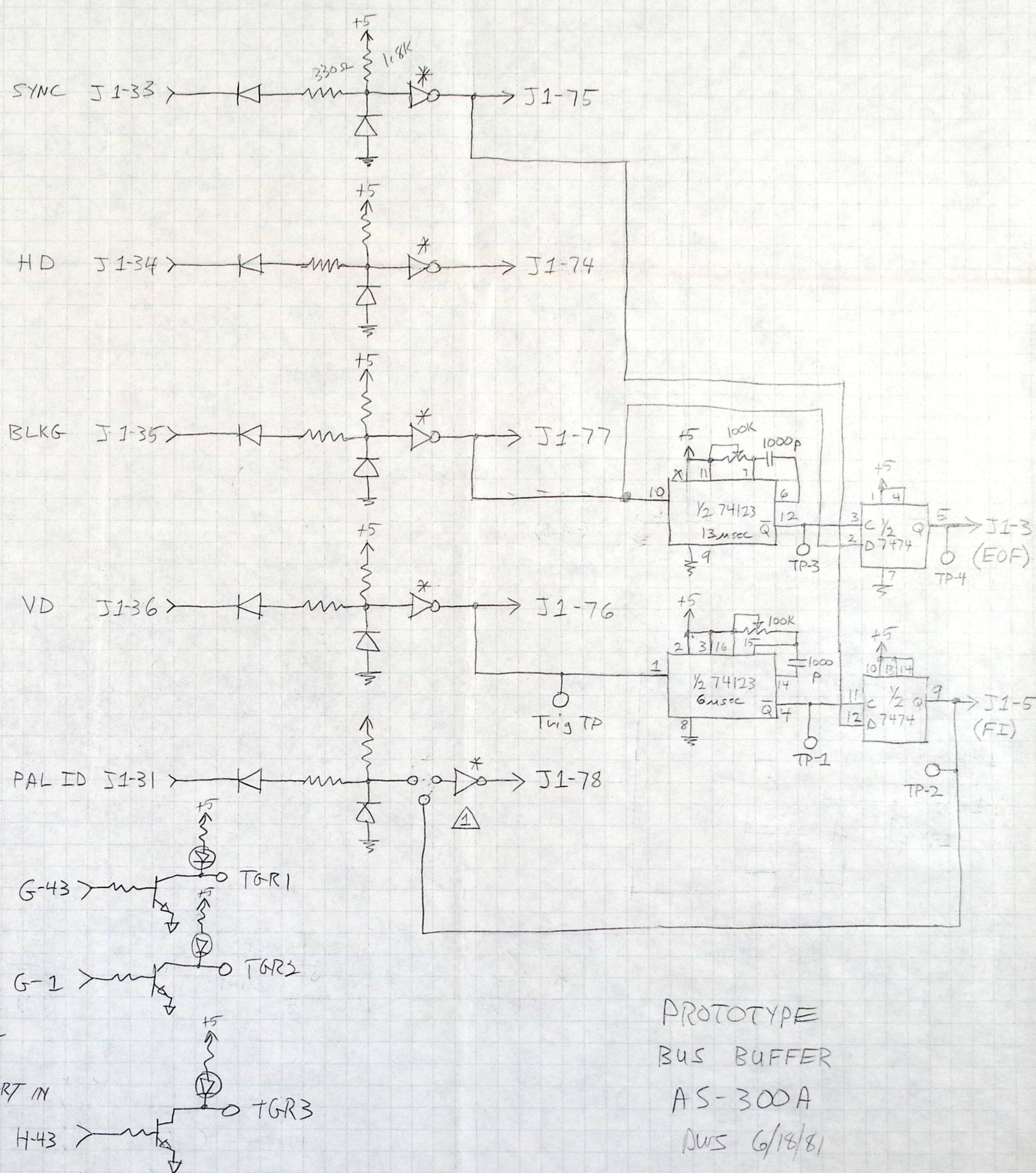
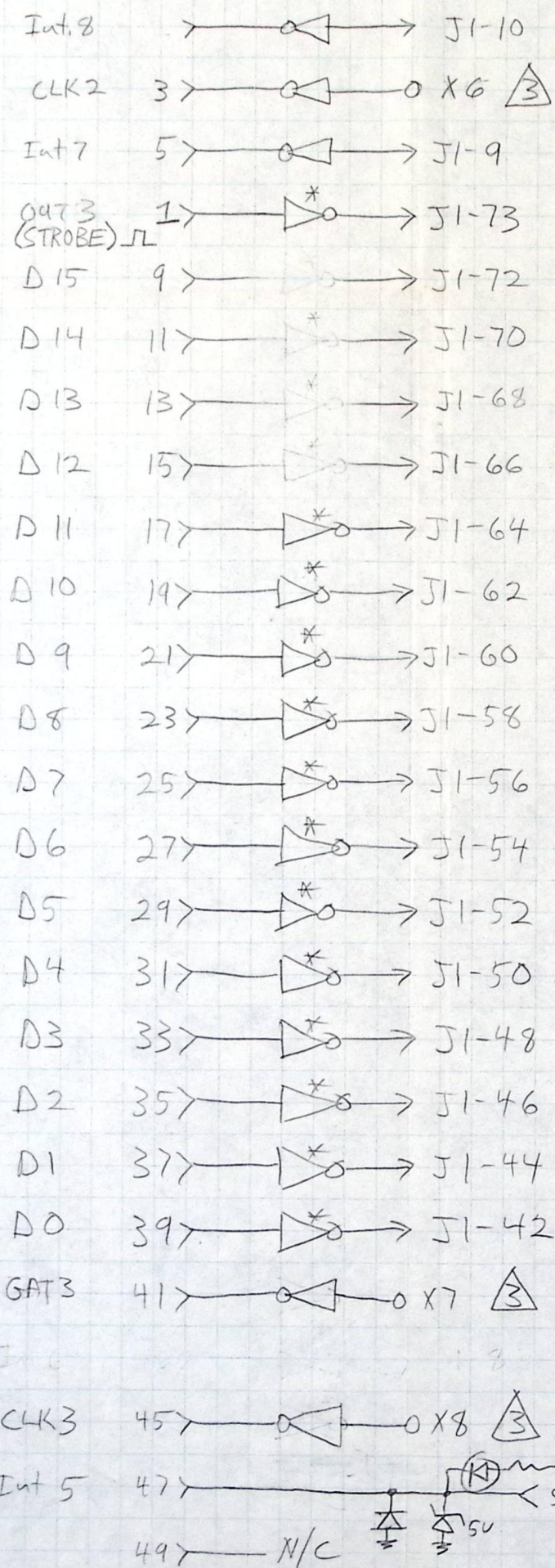




HEADER "G"  
ALL EVEN PIN # = GND

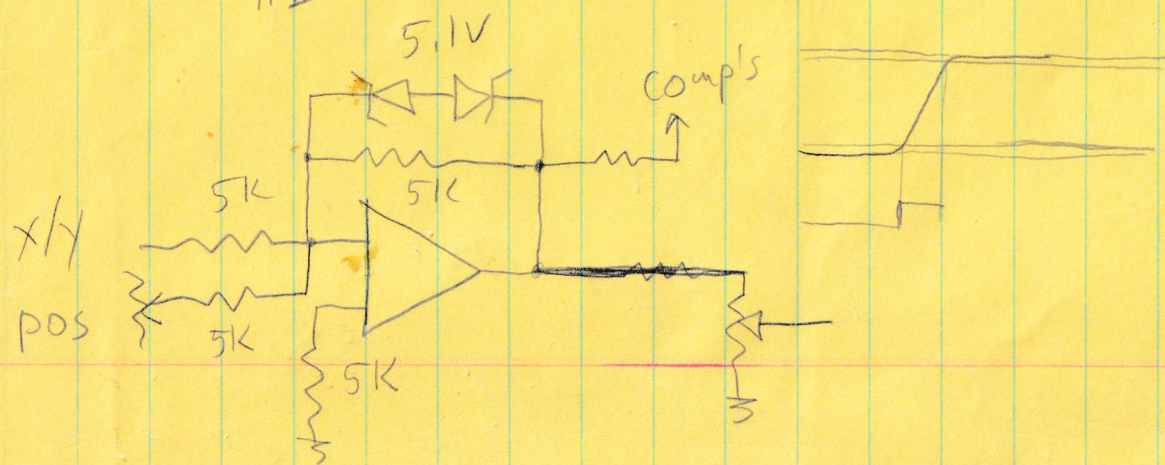
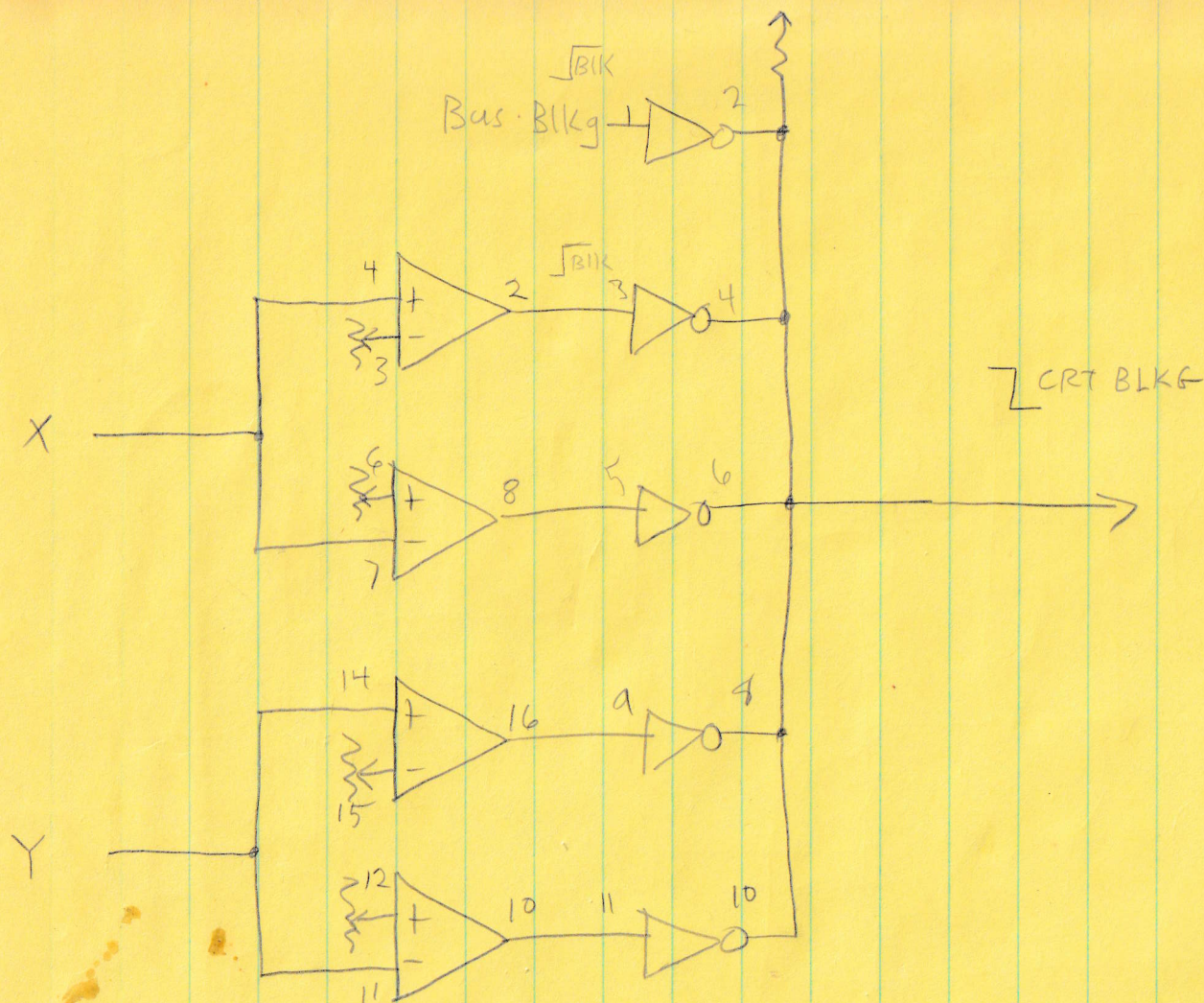


HEADER "H"  
ALL EVEN PIN # = GND



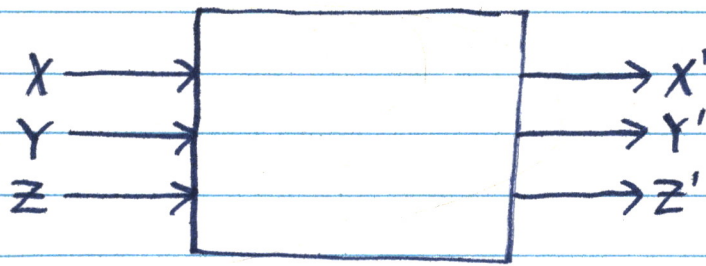
PROTOTYPE  
BUS BUFFER  
AS-300A  
DWS 6/18/81





CRT  
DRIVER





Arc Rotation:

$$X' = [X (\sin \phi')] + [Y (\cos \phi')]$$

$$Y' = [Y (\sin \phi')] - [X (\cos \phi')]$$

X Rotation:

$$Y' = [Y (\sin \phi'')] + [Z (\cos \phi'')]$$

$$Z' = [Z (\sin \phi'')] - [Y (\cos \phi'')]$$

Y Rotation:

$$X' = [X (\sin \phi''')] + [Z (\cos \phi''')]$$

$$Z' = [Z (\sin \phi''')] - [X (\cos \phi''')]$$

$$X' = [X (\sin \phi')] + [X (\sin \phi''')] + [Y (\cos \phi')] + [Z (\cos \phi''')]$$

$$Y' = [Y (\sin \phi')] + [Z (\sin \phi'')] + [X (\cos \phi')] + [Z (\cos \phi'')]$$

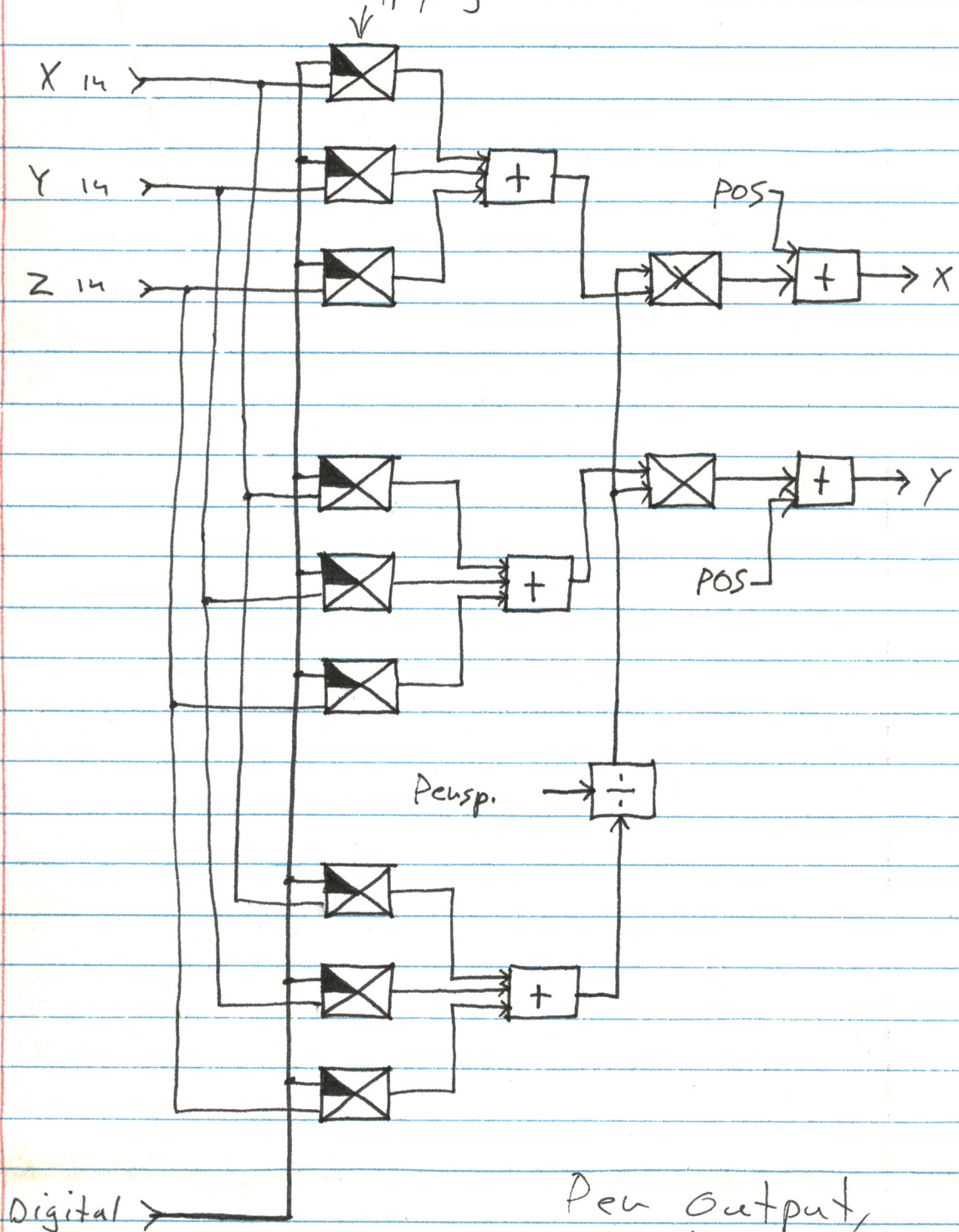
$$Z' = [Z (\sin \phi'')] + [Z (\sin \phi'')] - [Y (\cos \phi'')] - [X (\cos \phi''')]$$

$$X_{out} = X_{pos} + X' \left( \frac{P}{Z'} \right)$$

$$Y_{out} = Y_{pos} + Y' \left( \frac{P}{Z'} \right)$$



## Multiplying DAC's

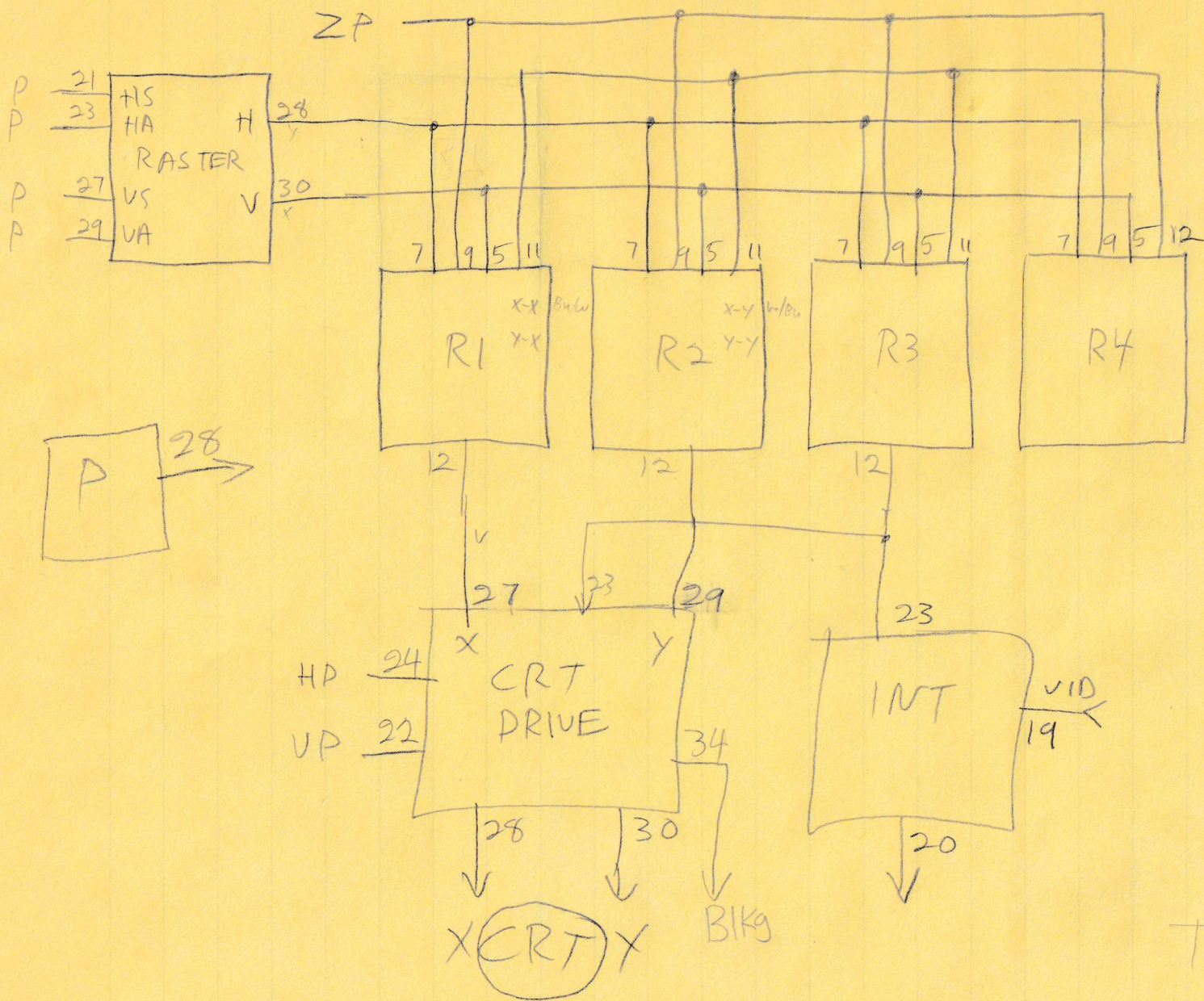


Pew Output,

- 1 Digital Multiply
- 1 Analog Multiply
- 2 Add's

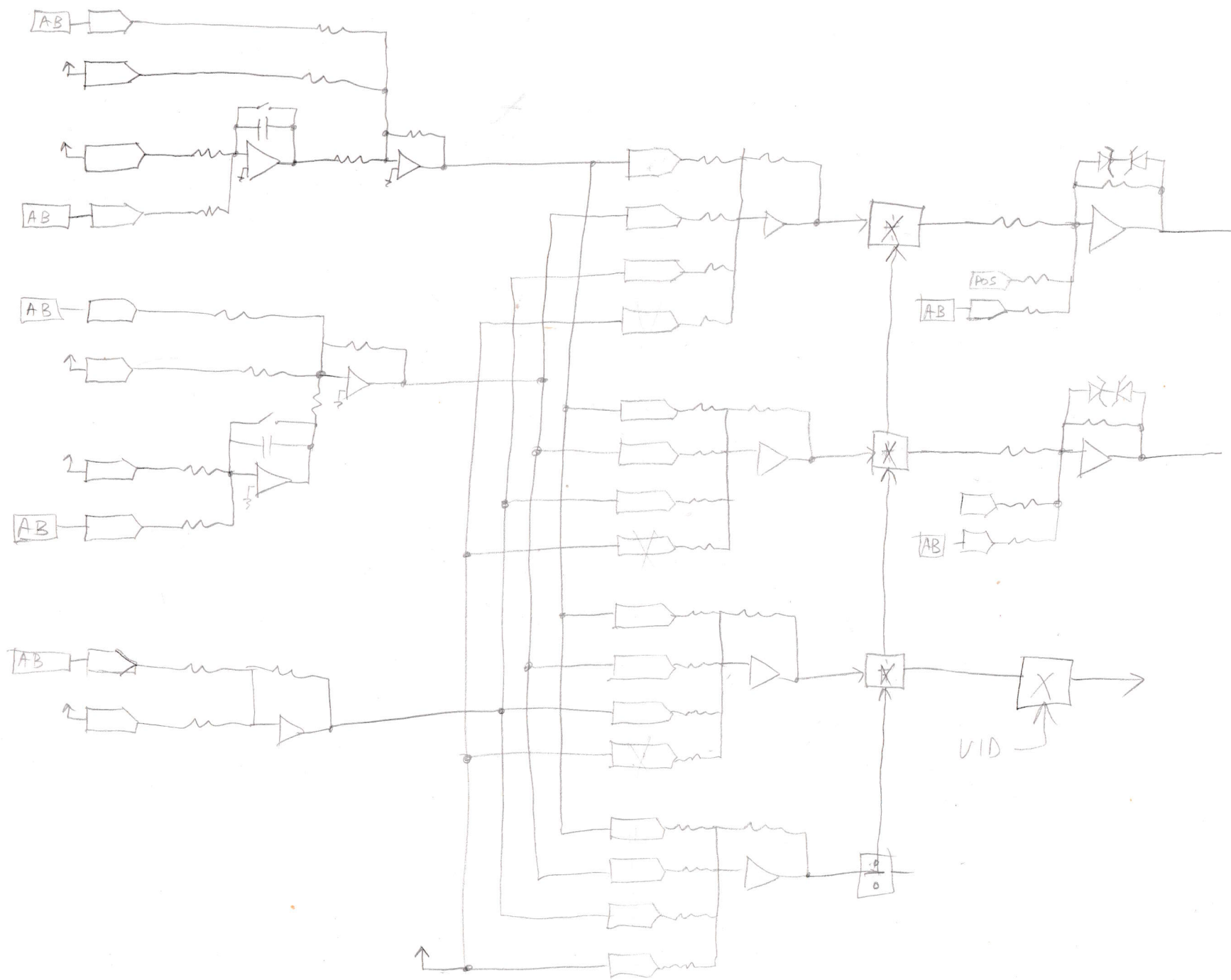
- 9 MDAC's
- 2 ~~MDAC's~~ Analog Mult,
- 1 Analog  $\div$
- 5 Add's





Test Chassis  
Interconnect



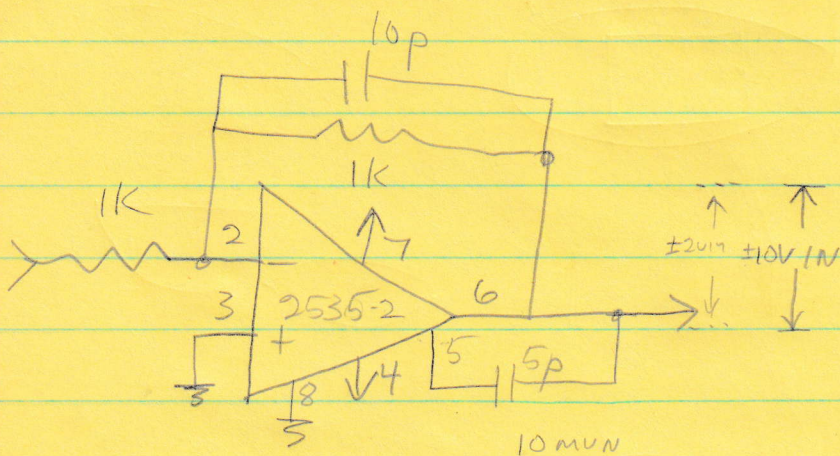




# 

Pricing-  
100's

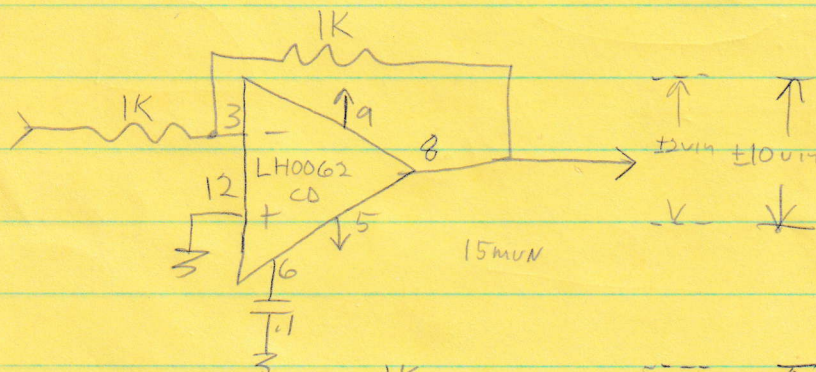
16.00



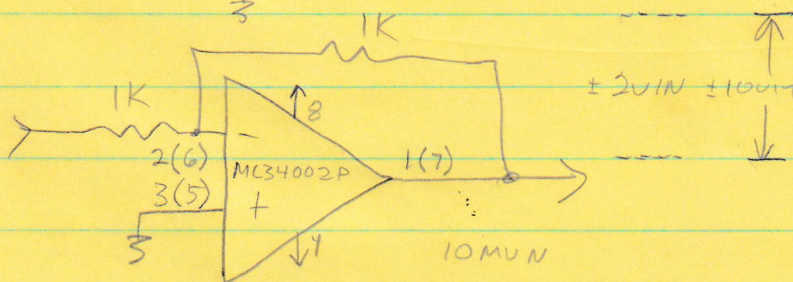
0 1m 5m 10mhz

17.85

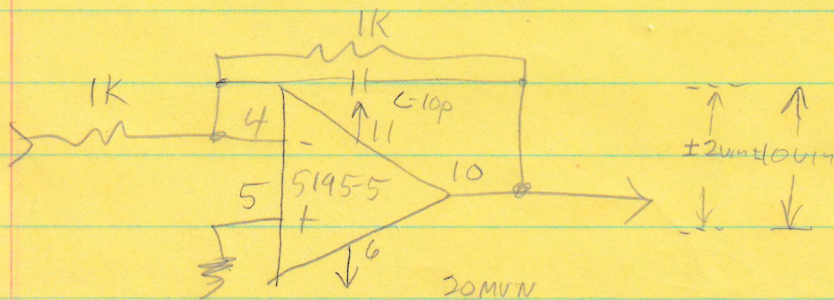
X



189



8.60



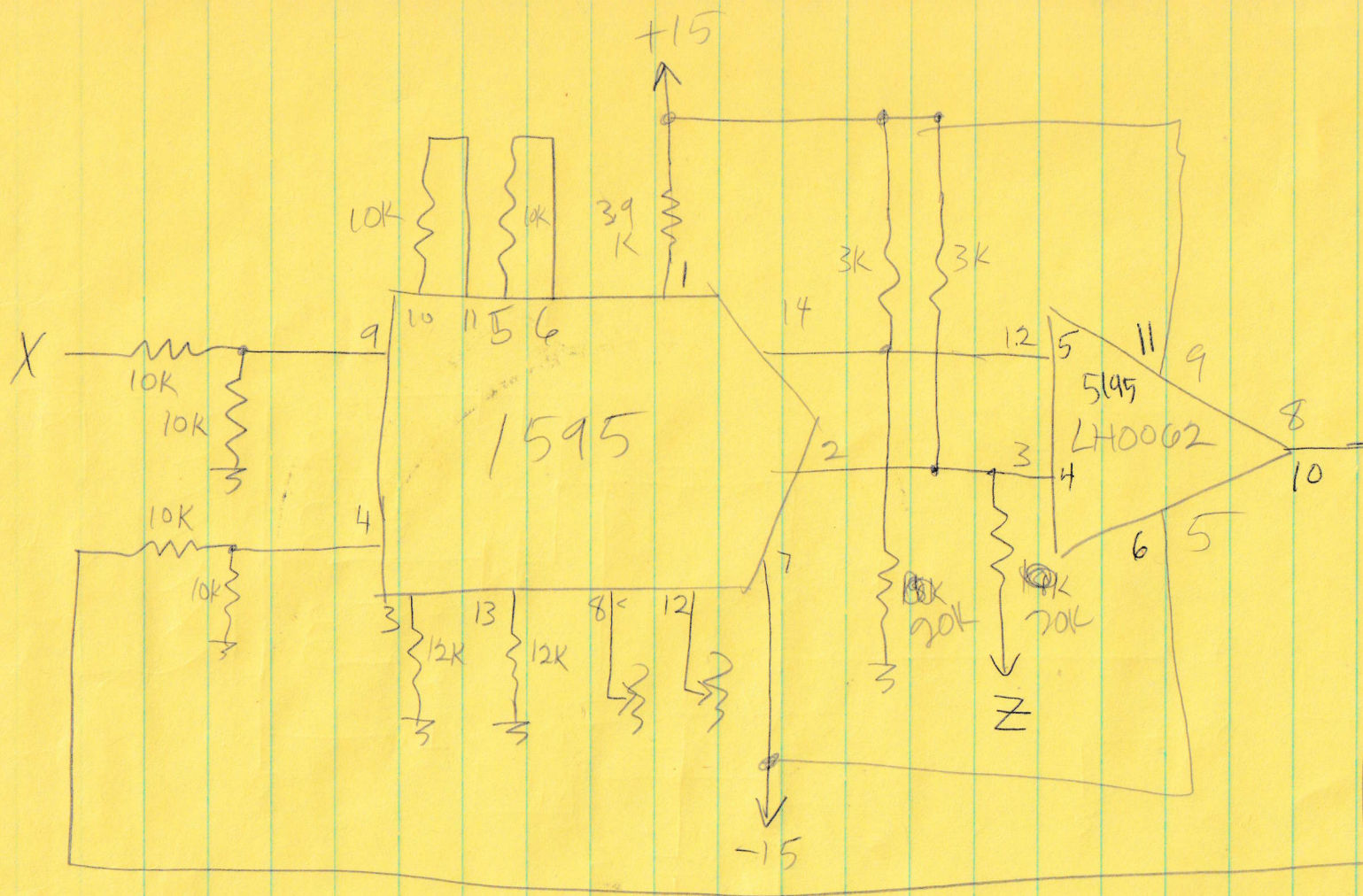
10p

20

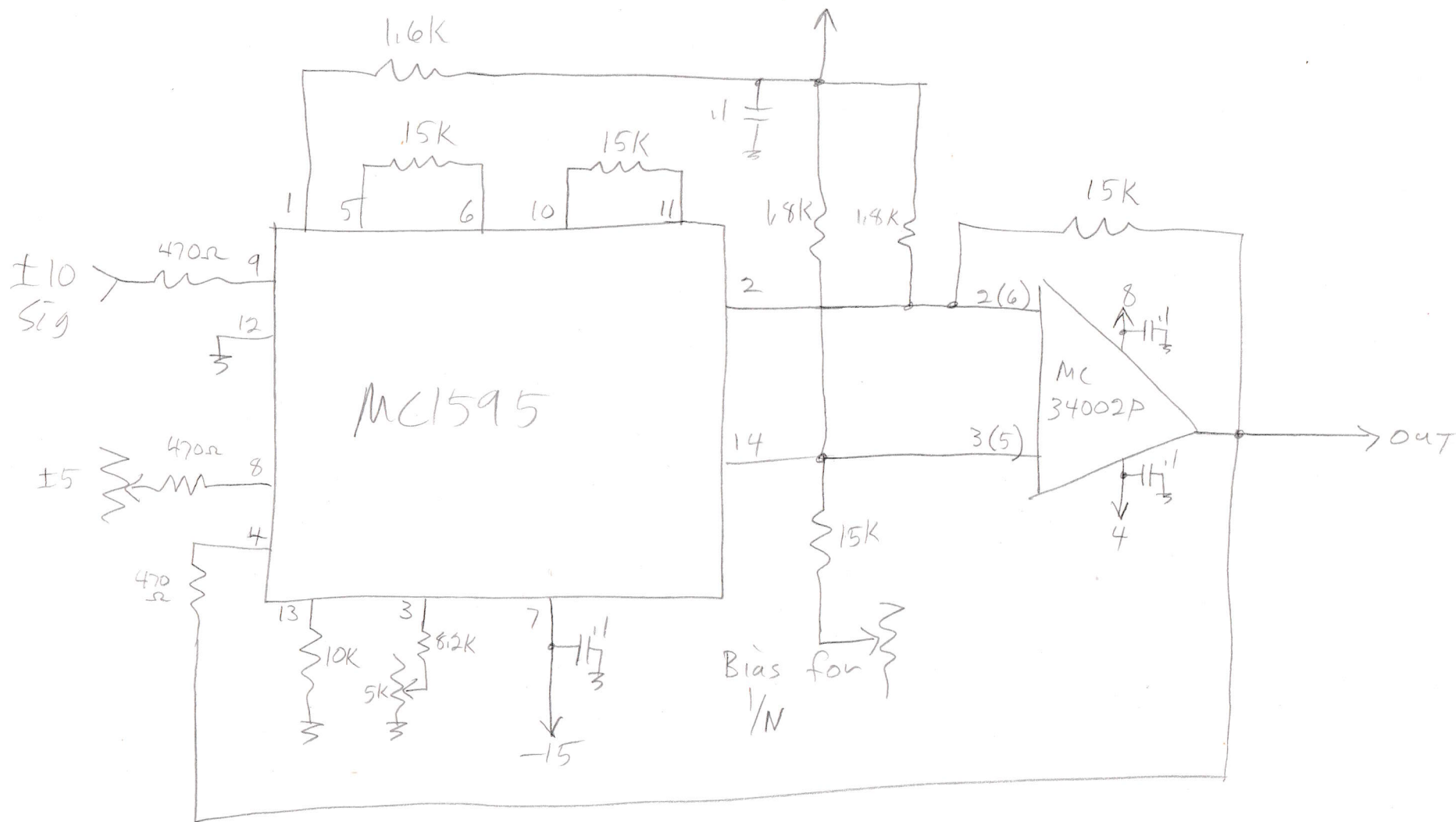










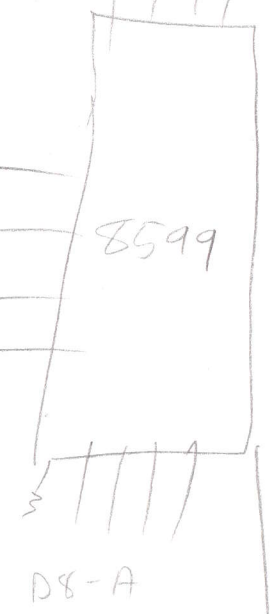
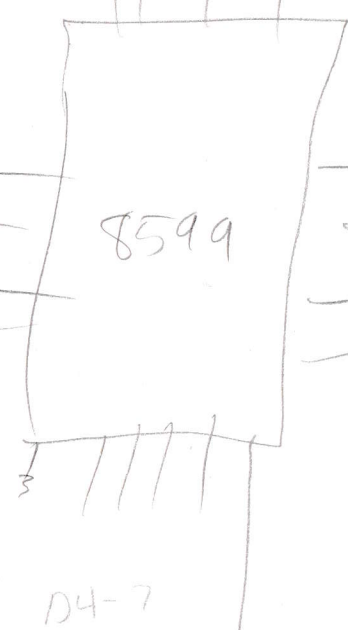
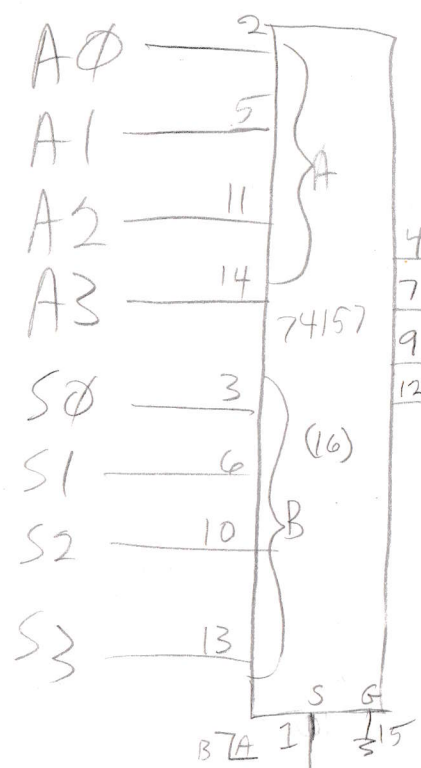
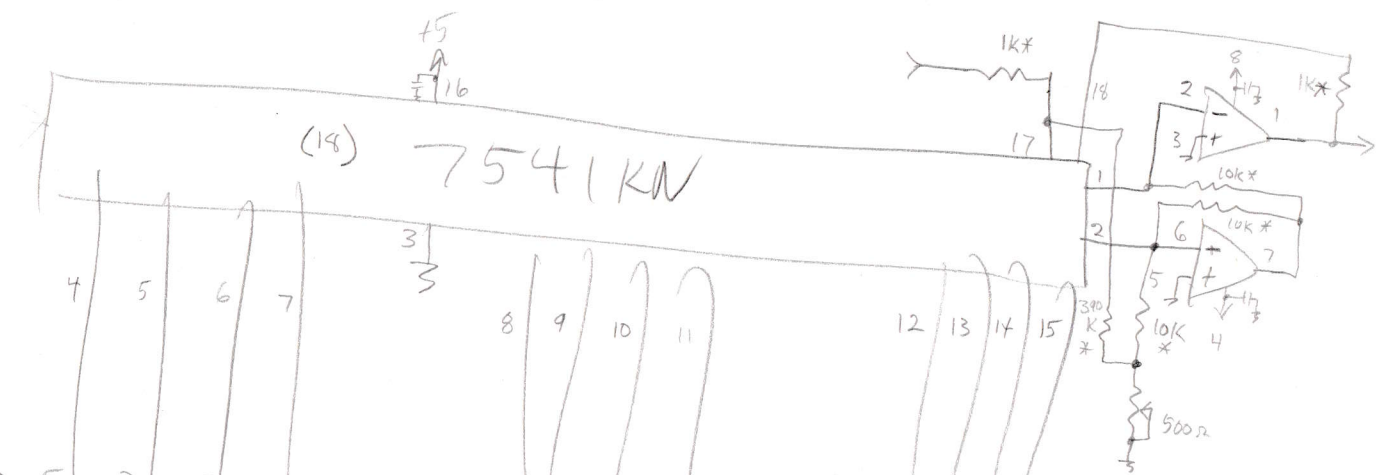


Low Noise 1/N

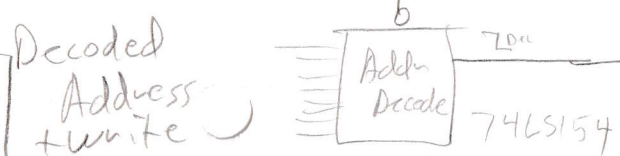
8-31-81 AWS



MC34002A

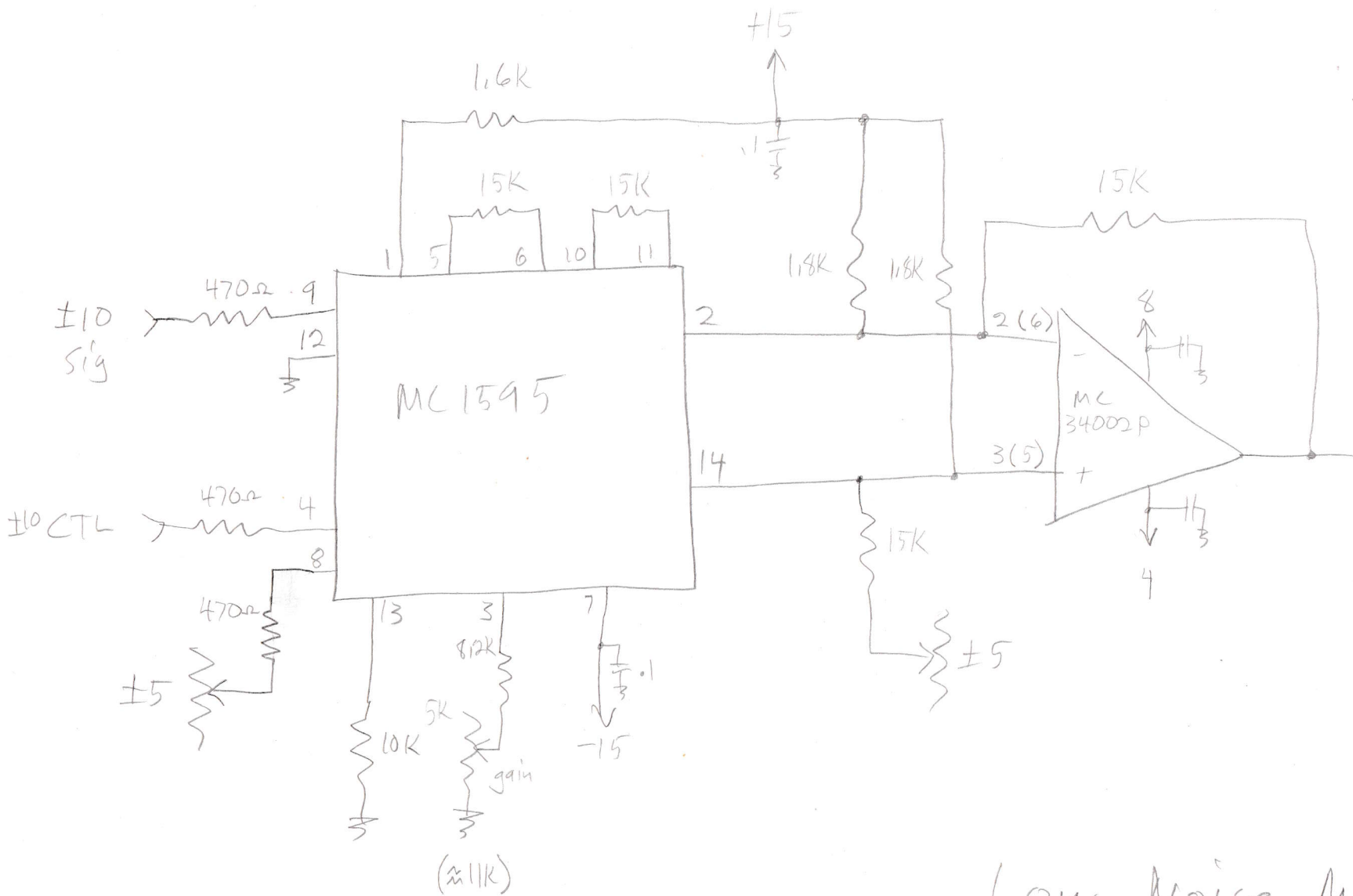


Vent  
Blkg



Hybrid Multiplier  
with Low Noise "off"  
8-28-81 DWS

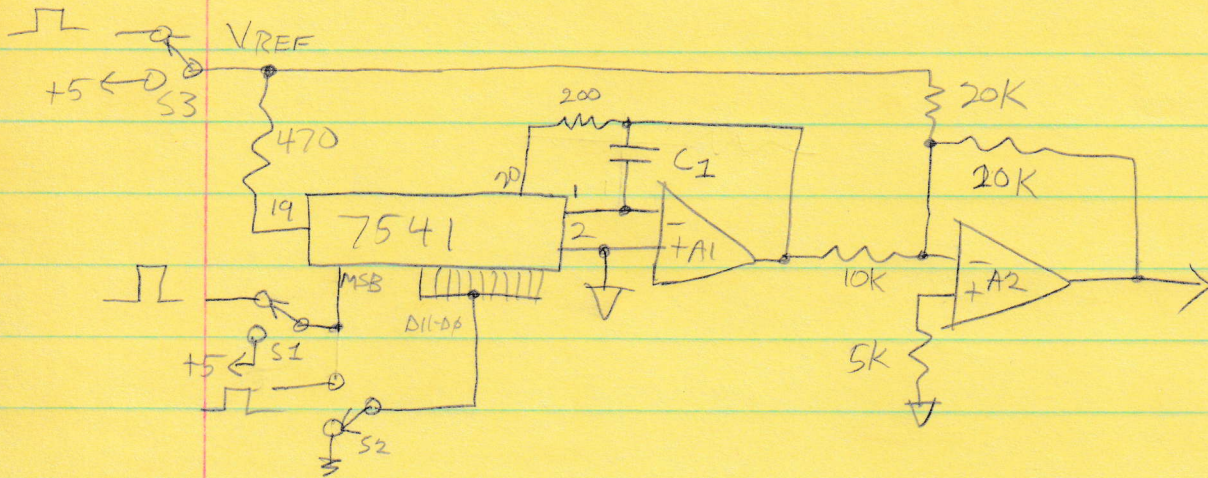




Low Noise Multiplier  
8-20-81 DWS

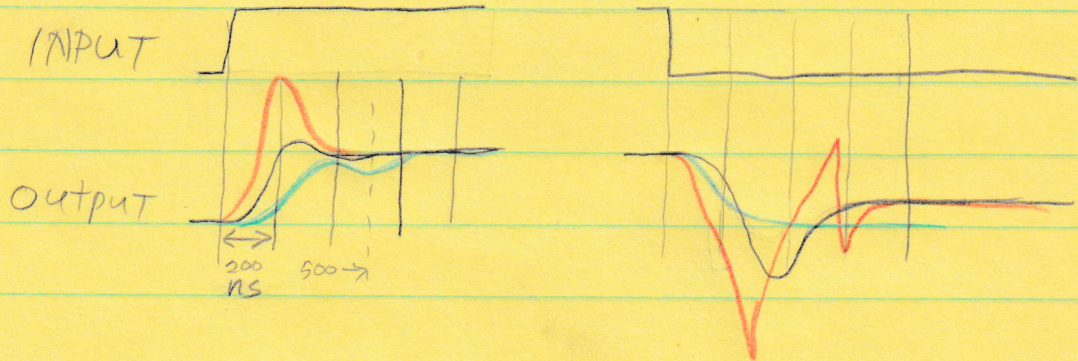


# Multiplying DAC

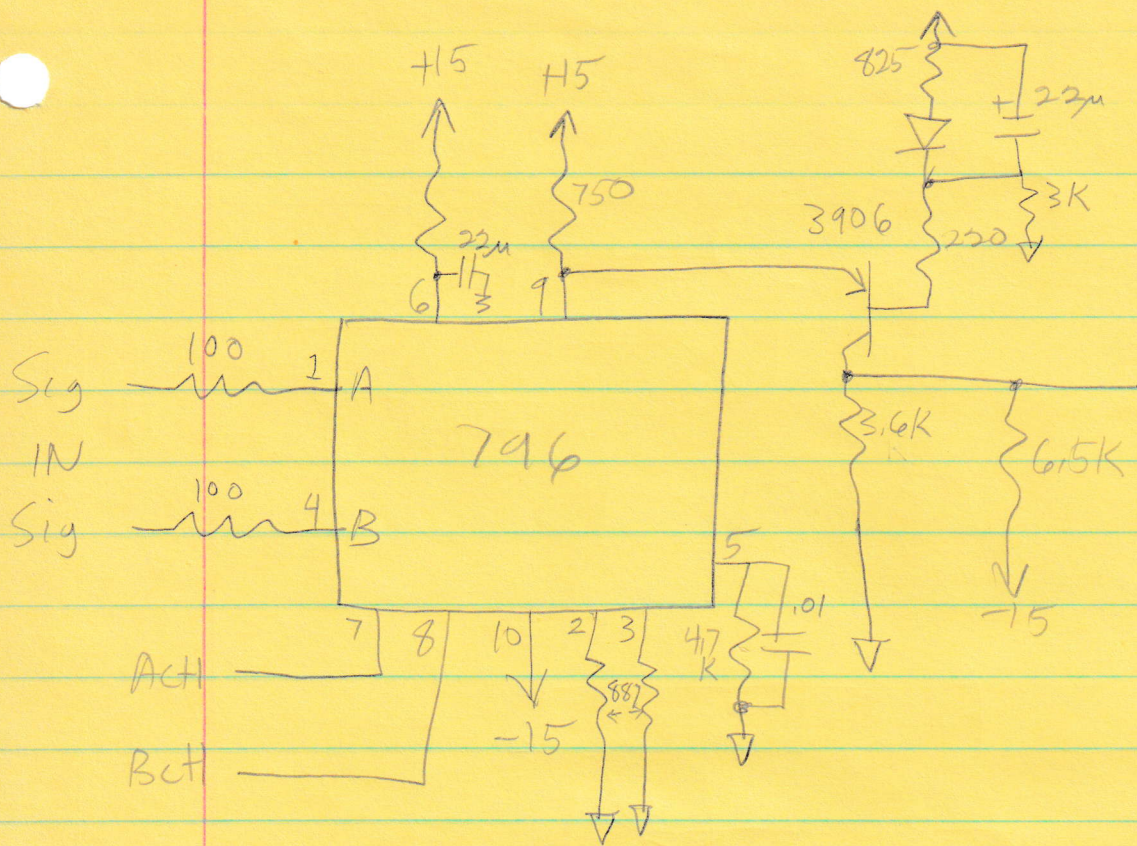


TEST!

5V to MSB  
 +5 to VREF  
 GND to D11-D0  
 C1 = 10pF  
 C1 = 40pF  
 C1 = 0pF

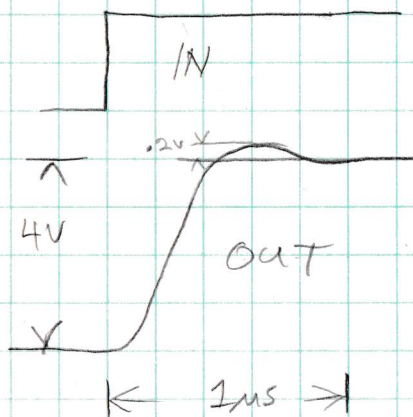
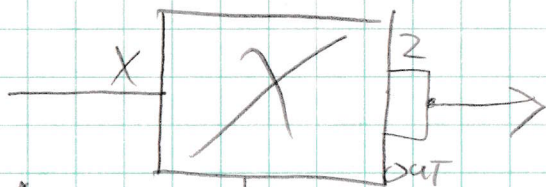




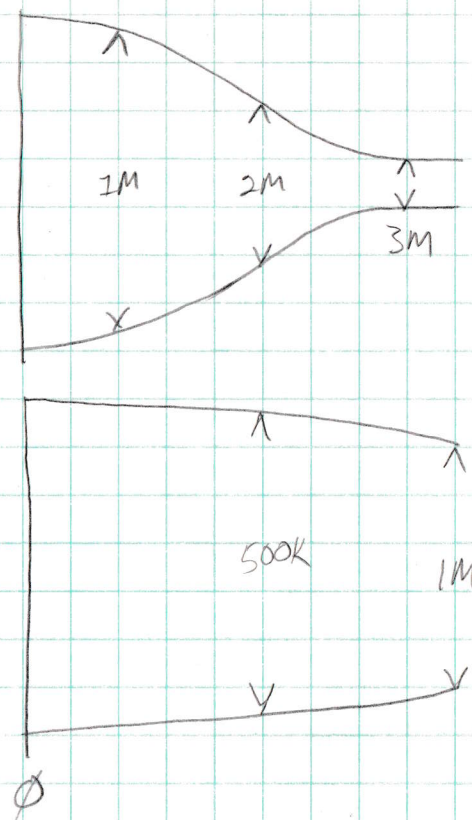




AD 533



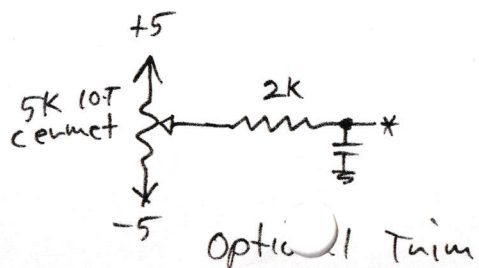
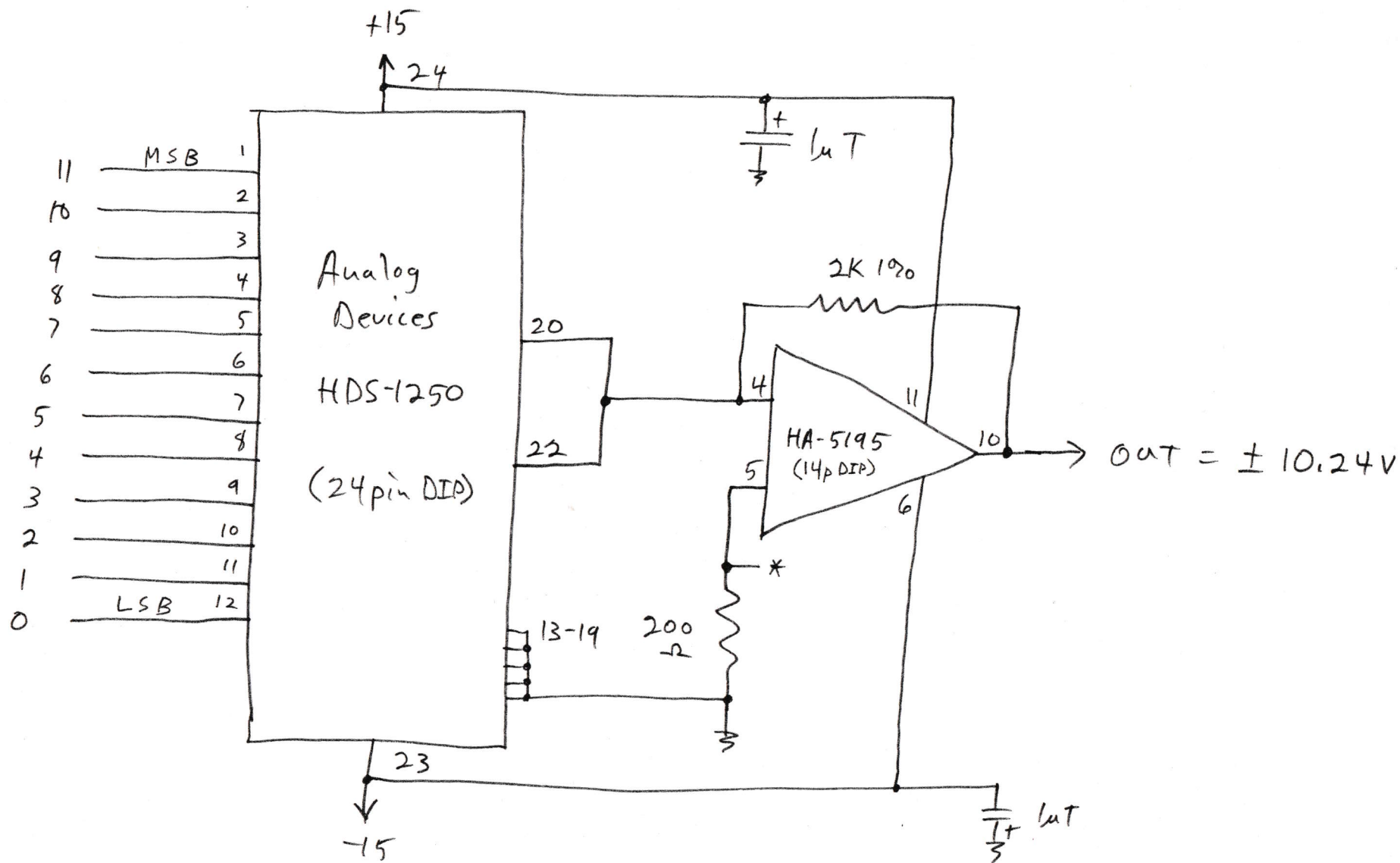
SWEEPS





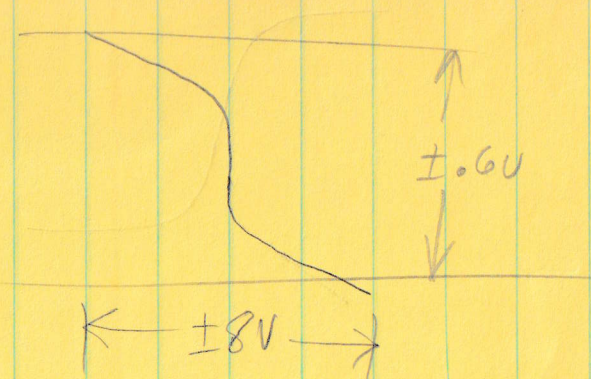






70 nsec DAC







## Super VersaBus

- \* 32 bit buffered Data
- \* 24 bit address
- \* 53 control
- \* Symmetric Timing

## Status Reg's

- Interrupt Masking
- Senses interrupt decides if response reqd.
- Mode register
- Front Panel

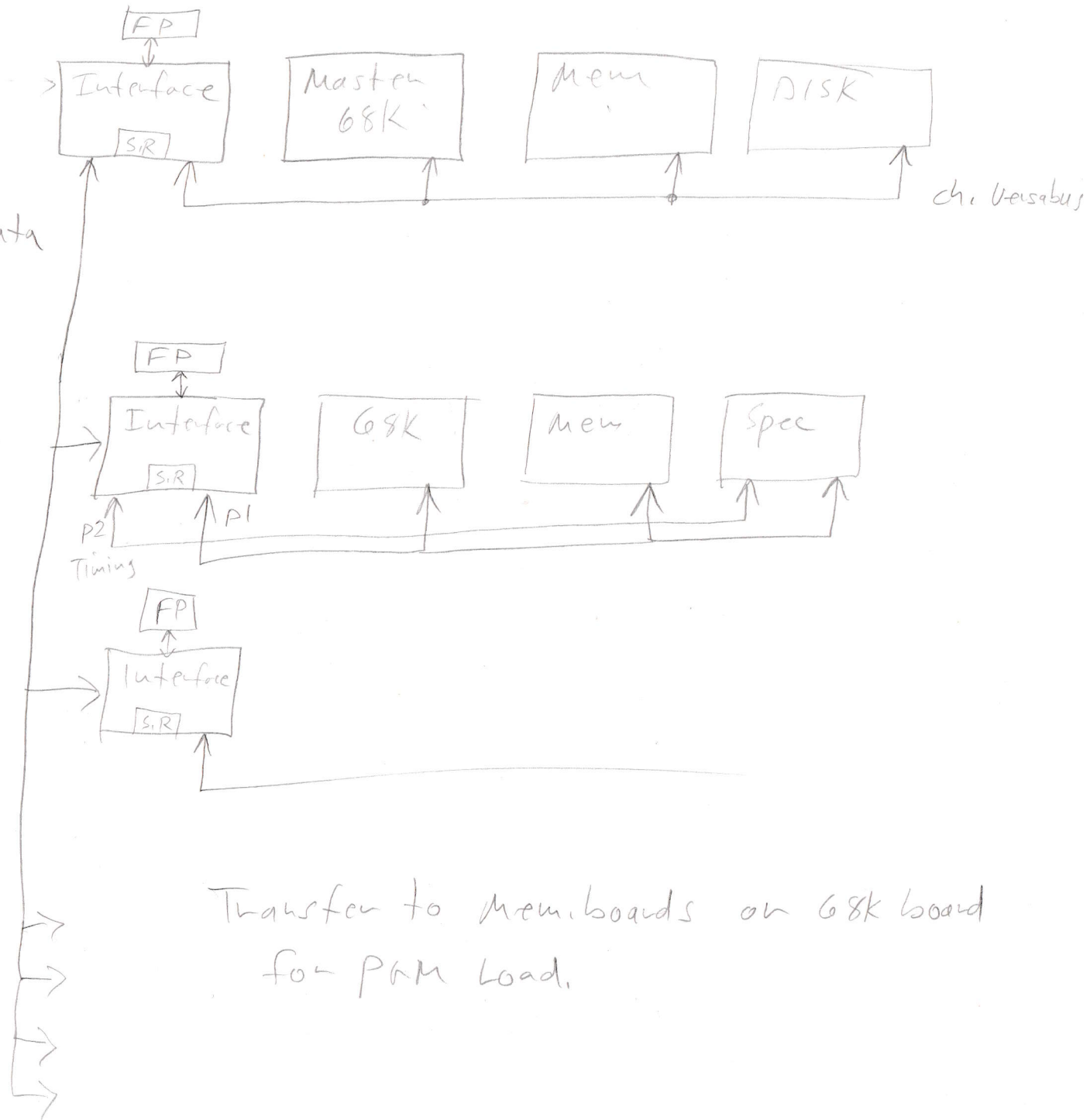




FIGURE 8-11. Standard Size PCB



TABLE 2. J2/P2 Pin Assignments

ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	+5V	8	+5V
9	+5V	10	+5V
11	+12V	12	+12V
13	GND ( $\pm$ 15V)	14	GND ( $\pm$ 15V)
15	-12V	16	-12V
17		18	
19		20	
21		22	
23		24	
25		26	
27		28	
29		30	
31		32	
33		34	
35		36	
37		38	
39		40	
41		42	
43		44	
45		46	
47		48	
49		50	
51		52	
53		54	
55		56	
57		58	
59		60	
61		62	
63		64	
65		66	
67	-15V	68	-15V
69	+15V	70	+15V
71		72	
73		74	
75		76	
77		78	
79		80	
81		82	
83		84	
85		86	
87		88	
89		90	
91		92	
93		94	
95		96	



TABLE 2. J2/P2 Pin Assignments for

(cont'd)

ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
97		98	
99		100	
101		102	
103		104	
105		106	
107		108	
109		110	
111		112	
113		114	
115		116	
117		118	
119		120	
NOTE: Pins 17 through 66 together by the backplane. are not bussed			



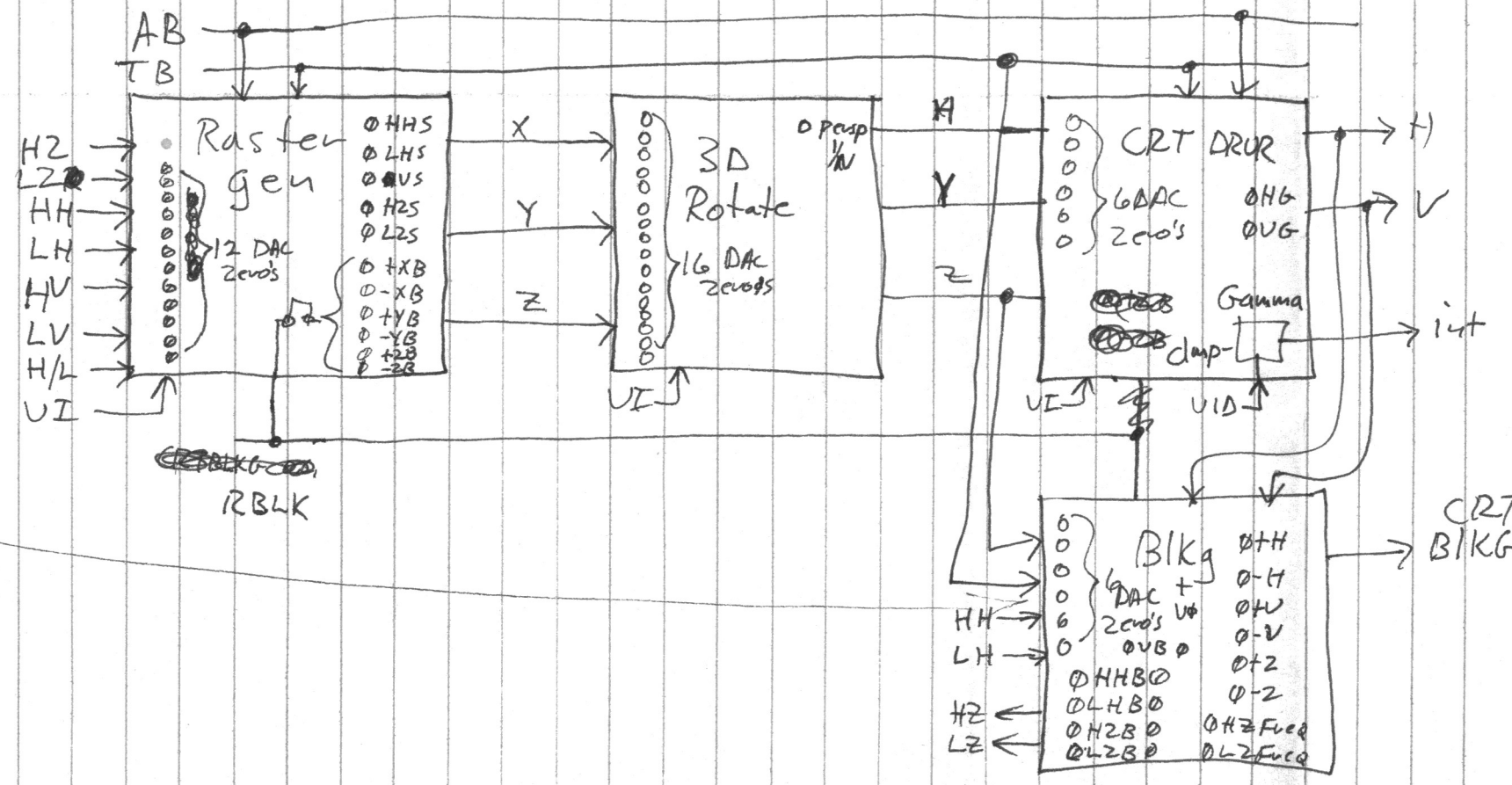
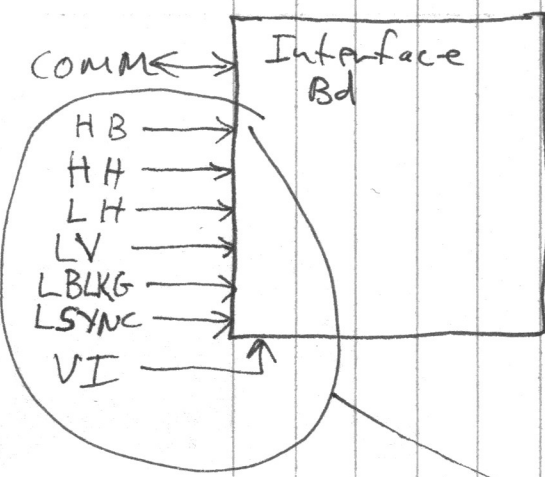
Board Name Raster Gen

Number VS-<sup>102</sup>~~100~~-A

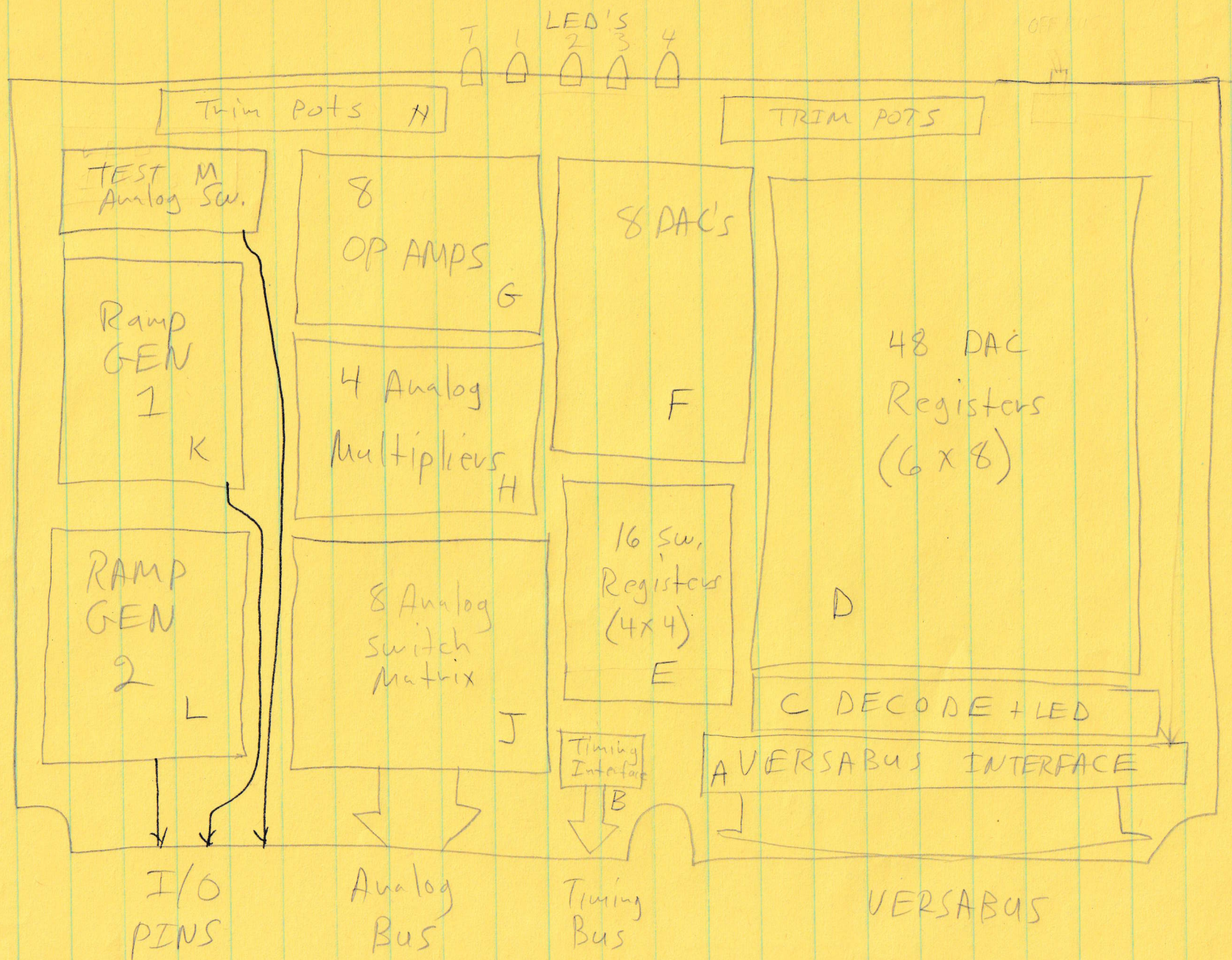
Base Address 0200 H

0200-020F	X size offset	(16 segments)
0210-021F	X Size Ampl.	"
0220-022F	X size Ext.	"
0230-023F	X Axis offset	"
0240-024F	X Axis Ampl.	"
0250-025F	X Axis Ext.	"
0260-026F	Y size offset	"
0270-027F	Y size Ampl.	"
0280-028F	Y size Ext	"
0290-029F	Y Axis offset	"
02A0-02AF	Y Axis Ampl	"
02B0-02BF	Y Axis Ext	"
02C0-02CF	Z size offset	"
02D0-02DF	Z size ampl.	"
02E0-02EF	Z size Ext.	"
02F0-02FF	Z axis offset	"
0300-030F	Z axis ampl	"
0310-031F	Z axis Ext	"
0320-03EF	Reserved	
03F0-03FF	Test Register	











# Versabus IO addresses

A8	A9	A10	A11	A12	A13	A14	A15	HEX	Assignment
0	0	0	0	0	0	0	0	00XX	Reserved
1	0	0	0	0	0	0	0	01XX	Raster + Axis
0	1	0	0	0	0	0	0	02XX	3-D Rotate
1	1	0	0	0	0	0	0	03XX	Depth + Persp.
0	0	1	0	0	0	0	0	04XX	Pos. + Intens.
1	0	1	0	0	0	0	0	05XX	Blkg.
0	1	1	0	0	0	0	0	06XX	Analog OSC
1	1	1	0	0	0	0	0	07XX	Analog funct
0	0	0	1	0	0	0	0	08XX	Colorize 1
1	0	0	1	0	0	0	0	09XX	Colorize 2
0	1	0	1	0	0	0	0	0AXX	Segment Control



Ifc



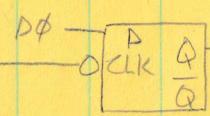
1A3 2A4 3A5

A6 4  
DS\* 5  
A7\* 6

CU3

15 EW1A  
14 EW2A  
13 EW1B  
12 EW2B  
11 EW3A  
10 EW4A  
9 EWT1  
7 EWS

} TO DU1-DU6  
} TO DU7-DU12  
} TO EU1-EU4  
TO M



NORM/HIRES

A7 4  
DS\* 5  
A6 6

CU4

15 EW1C  
14 EW2C  
13 EW1D  
12 EW2D  
11 EW3B  
10 EW4B  
9 EWT2

} TO DU13-DU18  
} TO DU19-DU24  
} TO EU5-EU8  
TO M

A6 4  
DS\* 5  
A7 6

CU5

15 EW1E  
14 EW2E  
13 EW1F  
12 EW2F  
11 EW3C  
10 EW4C  
9 EWT3

} TO DU25-DU30  
} TO DU31-DU36  
} TO EU9-EU12  
TO M

A7\* 4  
DS\* 5  
A6 6

CU6

15 EW1G  
14 EW2G  
13 EW1H  
12 EW2H  
11 EW3D  
10 EW4D  
9 EWT4

} TO DU37-DU42  
} TO DU43-DU48  
} TO EU13-EU16  
TO M

ID\*  
AS\*  
WR\*  
DS\*  
DS1\*

LS260

CU-1

NORM  
LO Addr  
Bits  
(A8\*)

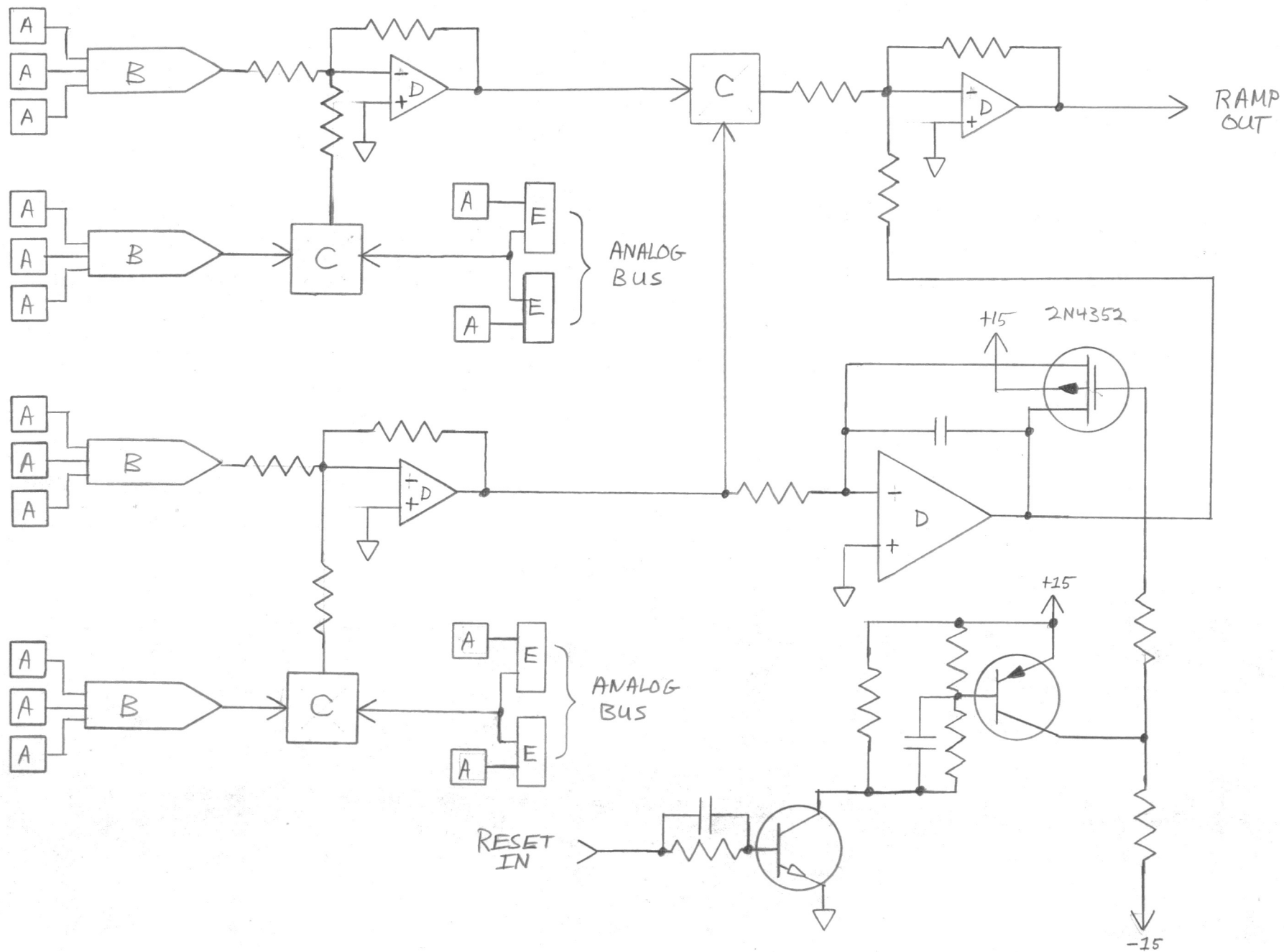
Norm Hi  
Addr  
Bits  
(A9\*-A15\*)

LS133

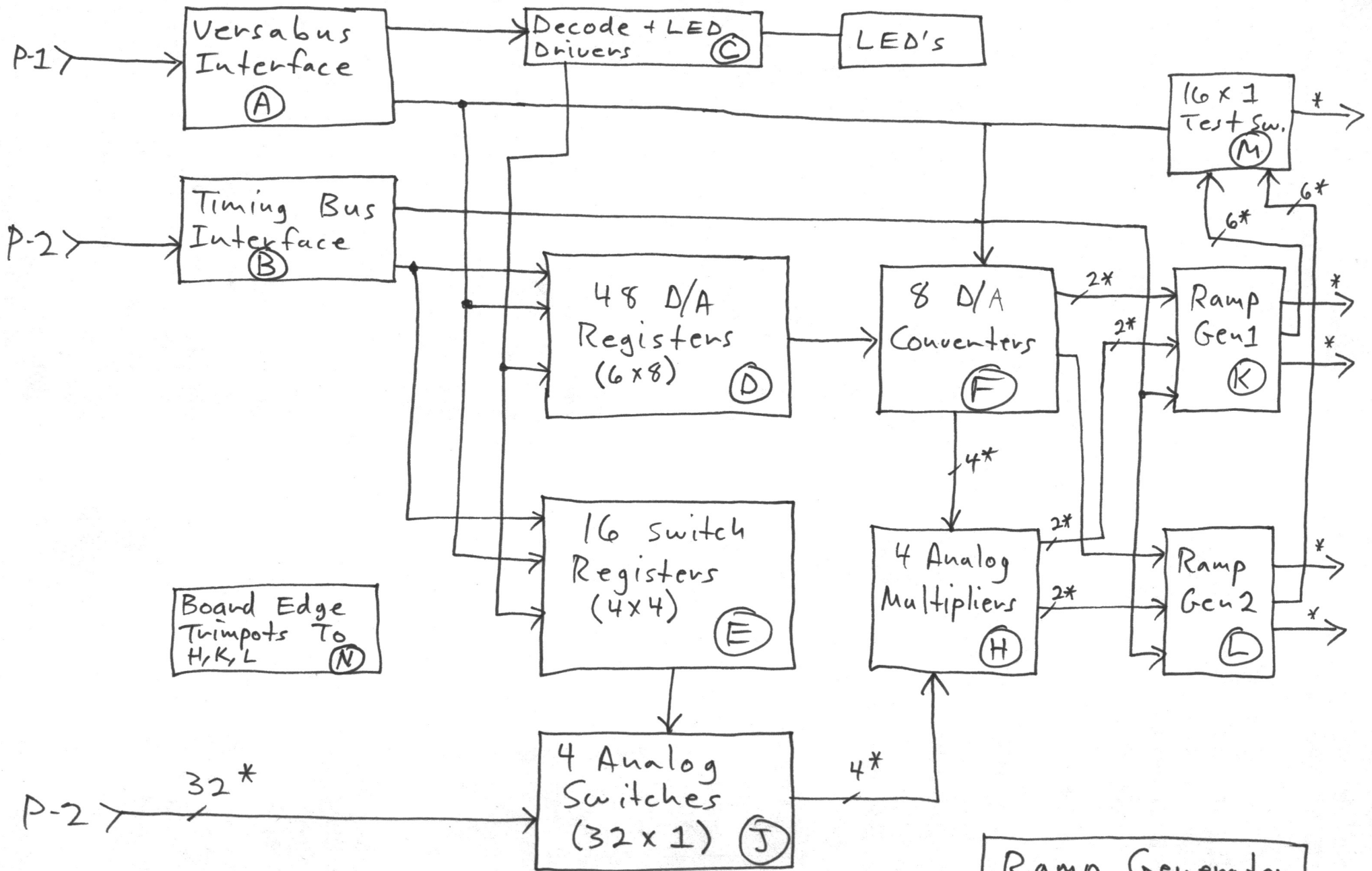
DS\*







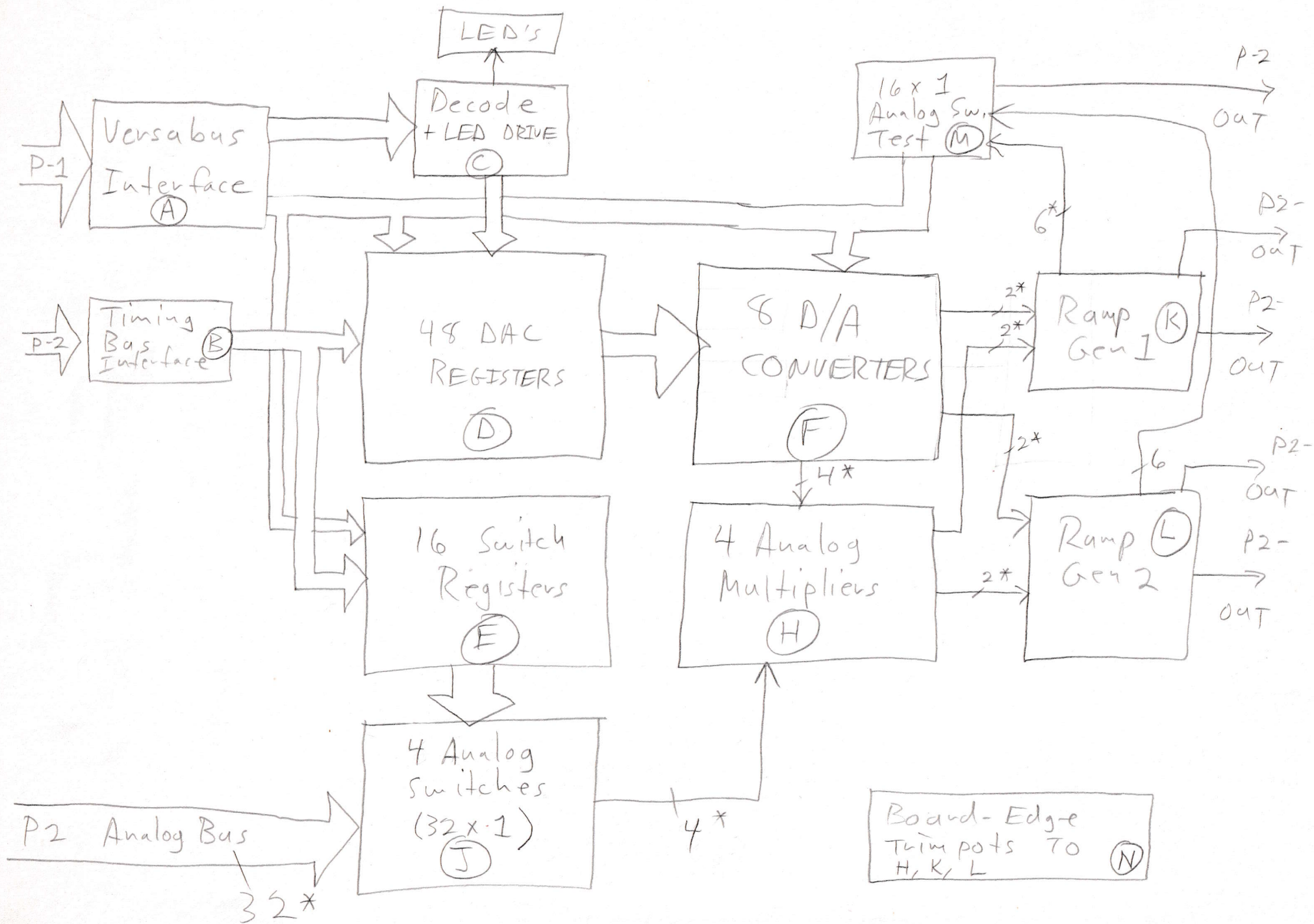




\* - Analog lines

Ramp Generator  
Block Diagram  
7/81 Dws







# Motorola Front Panel fig 7-2

LED's - 2 7seg Disp - 4bit in, LSA, MSD strobes

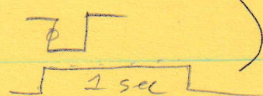
- 10 on/off

(6 - either/or)

user/supv

prim/sec

Rdy/fail

(1 - 1sec onr shot tgr by )

(2 - dedicated to

Ena/Disable pb+keysw.

## Switches

Pb - Co - Sys test

Sys Rst

S/W About

Sys Boot

Halt Recovery

Sec. Reset

Behind panel -

Pb - Dump

Keysw - Disable



BOARD NAME: RASTER AND AXIS  
BOARD NUMBER: VS-100A  
LAST REV. DATE: 6/10/81 D.W.S.  
ADDRESS ASSIGNMENTS:

PARAMETER	START ADDRESS (H)	# ADDRESSES
Hor. Size Bias	0100	8
Hor. Size Amp.	0110	8
Hor. Size Ext.	0120	8
Test 1	0130	1 (4)
Norm/Hi	013A	1 (4)
Hor. Axis Bias	0140	8
Hor. Axis Amp.	0150	8
Hor Axis Ext.	0160	8
Test 2	0170	0 (8)
Vent. Size Bias	0180	8
Vent. Size Amp.	0190	8
Vent. Size Ext.	01A0	8
Test 3	01B0	0 (8)
Vent. Axis Bias	01C0	8
vent. Axis Amp.	01D0	8
vent-Axis Ext.	01E0	8
Test 4	01F0	0 (8)



BOARD NAME: 3-D ROTATION

BOARD NUMBER: US-200A

LAST REV. DATE: 6/10/81 D.W.S.

ADDRESS ASSIGNMENTS:

PARAMETER	START ADDRESS (H)	#ADDRESSES
Pre-Rotation	0200	8
X Rotation	0210	8
Y Rotation	0220	8
Z Rotation	0230	8
Test	0240	1 (224)



BOARD NAME: DEPTH AND PERSPECTIVE

BOARD NUMBER: VS-300A

LAST REV. DATE: 6/10/81 D.W.S.

ADDRESS ASSIGNMENTS:

PARAMETER	START ADDRESS (H)	# ADDRESSES
Depth Bias	0300	8
Depth Amp. <sup>21</sup>	0310	8
Depth Ext.	0320	8
Test 1	0330	1 (8)
Focal Bias	0340	8
Focal Amp.	0350	8
Focal Ext.	0360	8
Test 2	0370	0 (8)
Z Bias	0380	8
Z Amp.	0390	8
Z Ext.	03A0	8
Test 3	03B0	0 (8)
Intensity Bias	03C0	8
Intensity Amp.	03D0	8
Intensity Ext.	03E0	8
Test 4	03F0	0 (8)



# SIGNAL CHARACTERISTICS, "BUS" CONNECTOR P1

CONNECTOR PIN	SIGNAL MNEMONIC	FUNCTIONAL DESCRIPTION	SIGNAL CHARACTERISTICS	
			INPUT	OUTPUT
1,2	+5V	+5 VOLTS DC POWER	(See VERSAbus Spec)	(See VERSAbus Spec)
3,4	GND	GROUND	(Note 1)	(Note 1)
5	D00*	DATA BIT 0	"	"
6	D01*	" " 1	"	"
7	D02*	" " 2	"	"
8	D03*	" " 3	"	"
9	D04*	" " 4	"	"
10	D05*	" " 5	"	"
11	D06*	" " 6	"	"
12	D07*	" " 7	"	"
13	D08*	" " 8	"	"
14	D09*	" " 9	"	"
15	D10*	" " 10	"	"
16	D11*	" " 11	"	"
17	D12*	" " 12	"	"
18	D13*	" " 13	"	"
19	D14*	" " 14	"	"
20	D15*	" " 15	"	"
21,22	---	(RESERVED)	"	"
23,24	GND	GROUND	"	"
25	DS0*	DATA STROBE 0	"	"
26	DS1*	DATA STROBE 1	"	"
27,28	GND	GROUND	"	"
29	DTACK*	DATA TRANSFER ACKNOWLEDGE	"	"
30	AS*	ADDRESS STROBE	"	"
31,32	GND	GROUND	"	"
33	---	(RESERVED)	"	"
34	WRITE*	READ/WRITE INDICATOR	"	"
35	---	(RESERVED)	"	"
36	A01*	ADDRESS BIT 1	"	"
37	A02*	" " 2	"	"
38	A03*	" " 3	"	"
39	A04*	" " 4	"	"
40	A05*	" " 5	"	"
41	A06*	" " 6	"	"
42	A07*	" " 7	"	"
43	A08*	" " 8	"	"
44	A09*	" " 9	"	"
45	A10*	" " 10	"	"
46	A11*	" " 11	"	"
47	A12*	" " 12	"	"
48	A13*	" " 13	"	"
49	A14*	" " 14	"	"
50	A15*	" " 15	"	"
51	A16*	" " 16	"	"
52	A17*	" " 17	"	"
53	A18*	" " 18	"	"

Note (1) - For electrical characteristics and additional information, refer to VERSAbus Specification Manual, M68KVBS (D1).



TABLE 2 - cont'd

CONNECTOR PIN	SIGNAL MNEMONIC	FUNCTIONAL DESCRIPTION	SIGNAL CHARACTERISTICS	
			INPUT	OUTPUT
54	A19*	ADDRESS BIT 19	(SEE VERSA- bus Spec)	(See VERSA- bus Spec)
55	A20*	" " 20		"
56	A21*	" " 21		"
57	A22*	" " 22		"
58	A23*	" " 23	"	"
59	AM4*	ADDRESS MODIFIER BIT 4	"	"
60	AM7*	ADDRESS MODIFIER BIT 7	"	"
61	GND	GROUND	"	"
62	GND	GROUND	"	"
63	AM3*	ADDRESS MODIFIER BIT 3	"	"
64, 65, 66	---	(RESERVED)	"	"
67, 68	GND	SIGNAL GROUND	"	"
69	ACCLK	POWER LINE FREQUENCY (AC CLOCK)	"	"
70	SYSCLK	16 MHz CLOCK	"	"
71, 72	GND	GROUND	"	"
73	---	(RESERVED)	"	"
74	SYSRESET*	SYSTEM RESET	"	"
75, 76, 77	---	(RESERVED)	"	"
78	ACFAIL*	AC INPUT POWER FAILURE	"	"
79	---	(RESERVED)	"	"
80	SYSFAIL*	SYSTEM FAIL	"	"
81	BERR*	BUS ERROR	"	"
82	---	(RESERVED)	"	"
83	AM0*	ADDRESS MODIFIER BIT 0	"	"
84	AM1*	ADDRESS MODIFIER BIT 1	"	"
85	AM2*	ADDRESS MODIFIER BIT 2	"	"
86	AM6*	ADDRESS MODIFIER BIT 6	"	"
87	IRQ1*	INTERRUPT REQUEST 1	"	"
88	IRQ2*	" " 2	"	"
89	IRQ3*	" " 3	"	"
90	IRQ4*	" " 4	"	"
91	IRQ5*	" " 5	"	"
92	IRQ6*	" " 6	"	"
93	IRQ7*	" " 7	"	"
94	AM5*	ADDRESS MODIFIER BIT 5	"	"
95	ACKIN*	ACKNOWLEDGE IN	"	"
96	ACKOUT*	ACKNOWLEDGE OUT	"	"
97	BG0IN*	BUS GRANT IN, #0	"	"
98	BG0OUT*	BUS GRANT OUT, #0	"	"
99	BG1IN*	BUS GRANT IN, #1	"	"
100	BG1OUT*	BUS GRANT OUT, #1	"	"
101	BG2IN*	BUS GRANT IN, #2	"	"
102	BG2OUT*	BUS GRANT OUT, #2	"	"
103	BG3IN*	BUS GRANT IN, #3	"	"
104	BG3OUT*	BUS GRANT OUT, #3	"	"



TABLE 2 - cont'd

CONNECTOR PIN	SIGNAL MNEMONIC	FUNCTIONAL DESCRIPTION	SIGNAL CHARACTERISTICS	
			INPUT	OUTPUT
105	BG4IN*	BUS GRANT IN, #4	(See VERSAbus Spec)	(See VERSAbus Spec)
106	BG4OUT*	BUS GRANT OUT, #4	"	"
107	BR0*	BUS REQUEST, #0	"	"
108	BR1*	BUS REQUEST, #1	"	"
109	BR2*	BUS REQUEST #2	"	"
110	BR3*	BUS REQUEST #3	"	"
111	BR4*	BUS REQUEST #4	"	"
112	BBSY*	BUS BUSY	"	"
113	BCLR*	BUS CLEAR	"	"
114	BREL*	BUS RELEASE	"	"
115	---	(RESERVED)	"	"
116	---	(RESERVED)	"	"
117	---	(RESERVED)	"	"
118	---	(RESERVED)	"	"
119,120	GND	GROUND	"	"
121,122	-12V	-12 VOLTS DC POWER	"	"
123,124	GND	GROUND	"	"
125,126	+12V	+12 VOLTS DC POWER	"	"
127,128	+12V	+12 VOLTS DC POWER	"	"
129,130	+5V	+5 VOLTS DC POWER	"	"
131,132	+5V	+5 VOLTS DC POWER	"	"
133,134	---	(RESERVED)	"	"
135-140	GND	GROUND	"	"



TABLE 3  
SIGNAL CHARACTERISTICS, I/O CONNECTOR P2

CONNECTOR PIN	SIGNAL MNEMONIC	FUNCTIONAL DESCRIPTION	SIGNAL CHARACTERISTICS	
			INPUT	OUTPUT
1-6	GND	GROUND	-	-
7-10	+5V	+5 VOLTS DC POWER	-	-
11,12	+12V	+12 VOLTS DC POWER	-	-
13,14	GND	GROUND	-	-
15,16	-12V	-12 VOLTS DC POWER	-	-
17	GND	GROUND	-	-
18	C1	PTM CLOCK 1 INPUT	C*	(N/A)
19	TXD1	TRANSMIT DATA, SERIAL PORT #1	E**	E
20	G1	PTM GATE 1 INPUT	D	(N/A)
21	RXD1	RECEIVED DATA, SERIAL PORT #1	E**	E
22	O1	PTM #1 OUTPUT	(N/A)	B
23	RTS1	REQUEST TO SEND, SERIAL PORT #1	E**	E
24	C2	PTM CLOCK 2 INPUT	D	(N/A)
25	CTS1	CLEAR TO SEND, SERIAL PORT #1	E**	E
26	G2	PTM GATE 2 INPUT	D	(N/A)
27	DSR1	DATA SET READY, SERIAL PORT #1	E**	E
28	O2	PTM #2 OUTPUT	(N/A)	B
29	GND	GROUND	-	-
30	RR+	RECEIVER READY +, SERIAL PORT #2 (RS422)	F	(N/A)
31	DCD1	DATA CARRIER DETECT, SERIAL PORT #1	E**	E
32	RR-	RECEIVER READY, SERIAL PORT #2 (RS422)	F	(N/A)
33	DTR1	DATA TERMINAL READY, SERIAL PORT #1	E**	E
34	TR+	TERMINAL READY +, SERIAL PORT #2 (RS422)	(N/A)	F
35		(UNUSED)	-	-
36	TR-	TERMINAL READY -, SERIAL PORT #2 (RS422)	(N/A)	F
37		(UNUSED)	-	-
38	DM+	DATA MODE +, SERIAL PORT #2 (RS422)	F	(N/A)
39	O3	PTM #3 OUTPUT	(N/A)	B
40	DM-	DATA MODE -, SERIAL PORT #2 (RS422)	F	(N/A)
41	G3	PTM GATE 3 INPUT	D	(N/A)
42	CS+	CLEAR TO SEND +, SERIAL PORT #2 (RS422)	F	(N/A)

\*Signal categories are defined following this table.

\*\*Input/Output characteristics vary depending on whether this port is defined as a Terminal or Modem.



TABLE 3 - cont'd  
SIGNAL CHARACTERISTICS, I/O CONNECTOR P2

CONNECTOR PIN	SIGNAL MNEMONIC	FUNCTIONAL DESCRIPTION	SIGNAL CHARACTERISTICS	
			INPUT	OUTPUT
43	C3	PTM CLOCK 3 INPUT	D*	(N/A)
44	CS-	CLEAR TO SEND -, SERIAL PORT #2 (RS422)	F	(N/A)
45	GND	GROUND	-	-
46	RT+	RECEIVE TIMING +, SERIAL PORT #2 (RS422)	F	(N/A)
47	TXD2	TRANSMIT DATA, SERIAL PORT #2 (RS232C)	E**	E
48	RT-	RECEIVE TIMING -, SERIAL PORT #2 (RS422)	F	(N/A)
49	RXD2	RECEIVED DATA, SERIAL PORT #2 (RS232C)	E**	E
50	RS+	REQUEST TO SEND +, SERIAL PORT #2 (RS422)	(N/A)	F
51	RTS2	REQUEST TO SEND, SERIAL PORT #2 (RS232C)	E**	E
52	RS-	REQUEST TO SEND -, SERIAL PORT #2 (RS422)	(N/A)	F
53	CTS2	CLEAR TO SEND, SERIAL PORT #2 (RS232C)	E**	E
54	RD+	RECEIVE DATA +, SERIAL PORT #2 (RS422)	F	(N/A)
55	DSR2	DATA SET READY, SERIAL PORT #2 (RS232C)	E**	E
56	RD-	RECEIVE DATA -, SERIAL PORT #2 (RS422)	F	(N/A)
57	GND	GROUND	-	-
58	ST+	SEND TIMING +, SERIAL PORT #2 (RS422)	F	(N/A)
59	DCD2	DATA CARRIER DETECT, SERIAL PORT #2 (RS232C)	E**	E
60	ST-	SEND TIMING -, SERIAL PORT #2 (RS422)	F	(N/A)
61	DTR2	DATA TERMINAL READY, SERIAL PORT #2 (RS232C)	E**	E
62	SD+	SEND DATA +, SERIAL PORT #2 (RS422)	(N/A)	F
63	RXC2	RECEIVE DATA CLOCK, SERIAL PORT #2 (RS232C)	E**	E
64	SD-	SEND DATA -, SERIAL PORT #2 (RS422)	(N/A)	F
65	TXC2	TRANSMIT DATA CLOCK, SERIAL PORT #2 (RS232C)	E**	E
66	GND	GROUND	-	-
67-70		(UNUSED)	-	-
71	P1CB2	PARALLEL PORT 1, CB2 CONTROL LINE	(N/A)	B

\*Signal categories are defined following this table.

\*\*Input/Output characteristics vary depending on whether this port is defined as a Terminal or Modem.



TABLE 3 - cont'd  
SIGNAL CHARACTERISTICS, I/O CONNECTOR P2

CONNECTOR PIN	SIGNAL MNEMONIC	FUNCTIONAL DESCRIPTION	SIGNAL CHARACTERISTICS	
			INPUT	OUTPUT
72,73	GND	GROUND	-	-
74	P2CA1	PARALLEL PORT 2, CA1 CONTROL LINE	B*	(N/A)
75	P1CB1	PARALLEL PORT 1, CB1 CONTROL LINE	B	(N/A)
76,77	GND	GROUND	-	-
78	P2CA2	PARALLEL PORT 2, CA2 CONTROL LINE	(N/A)	B
79	P1PB7	PARALLEL PORT 1, UPPER DATA BYTE, BIT #7	A	A
80	GND	GROUND	-	-
81	P1PB6	PARALLEL PORT 1, UPPER DATA BYTE, BIT #6	A	A
82	P2PA0	PARALLEL PORT 2, LOWER DATA BYTE, BIT #0	A	A
83	P1PB5	PARALLEL PORT 1, UPPER DATA BYTE, BIT #5	A	A
84	P2PA1	PARALLEL PORT 2, LOWER DATA BYTE, BIT #1	A	A
85	P1PB4	PARALLEL PORT 1, UPPER DATA BYTE, BIT #4	A	A
86	P2PA2	PARALLEL PORT 2, LOWER DATA BYTE, BIT #2	A	A
87	P1PB3	PARALLEL PORT 1, UPPER DATA BYTE, BIT #3	A	A
88	P2PA3	PARALLEL PORT 2, LOWER DATA BYTE, BIT #3	A	A
89	P1PB2	PARALLEL PORT 1, UPPER DATA BYTE, BIT #2	A	A
90	P2PA4	PARALLEL PORT 2, LOWER DATA BYTE, BIT #4	A	A
91	P1PB1	PARALLEL PORT 1, UPPER DATA BYTE, BIT #1	A	A
92	P2PA5	PARALLEL PORT 2, LOWER DATA BYTE, BIT #5	A	A
93	P1PB0	PARALLEL PORT 1, UPPER DATA BYTE, BIT #0	A	A
94	P2PA6	PARALLEL PORT 2, LOWER DATA BYTE, BIT #6	A	A
95	P1PA7	PARALLEL PORT 1, LOWER DATA BYTE, BIT #7	A	A
96	P2PA7	PARALLEL PORT 2, LOWER DATA BYTE, BIT #7	A	A
97	P1PA6	PARALLEL PORT 1, LOWER DATA BYTE, BIT #6	A	A
98	P2PB0	PARALLEL PORT 2, UPPER DATA BYTE, BIT #0	A	A

\*Signal categories are defined following this table.



TABLE 3 - cont'd  
SIGNAL CHARACTERISTICS, I/O CONNECTOR P2

CONNECTOR PIN	SIGNAL MNEMONIC	FUNCTIONAL DESCRIPTION	SIGNAL CHARACTERISTICS	
			INPUT	OUTPUT
99	P1PA5	PARALLEL PORT 1, LOWER DATA BYTE, BIT #5	A*	A
100	P2PB1	PARALLEL PORT 2, UPPER DATA BYTE, BIT #1	A*	A
101	P1PA4	PARALLEL PORT 1, LOWER DATA BYTE, BIT #4	A*	A
102	P2PB2	PARALLEL PORT 2, UPPER DATA BYTE, BIT #2	A*	A
103	P1PA3	PARALLEL PORT 1, LOWER DATA BYTE, BIT #3	A*	A
104	P2PB3	PARALLEL PORT 2, UPPER DATA BYTE, BIT #3	A*	A
105	P1PA2	PARALLEL PORT 1, LOWER DATA BYTE, BIT #2	A*	A
106	P2PB4	PARALLEL PORT 2, UPPER DATA BYTE, BIT #4	A*	A
107	P1PA1	PARALLEL PORT 1, LOWER DATA BYTE, BIT #1	A*	A
108	P2PB5	PARALLEL PORT 2, UPPER DATA BYTE, BIT #5	A*	A
109	P1PA0	PARALLEL PORT 1, LOWER DATA BYTE, BIT #0	A*	A
110	P2PB6	PARALLEL PORT 2, UPPER DATA BYTE, BIT #6	A	A
111	GND	GROUND	-	-
112	P2PB7	PARALLEL PORT 2, UPPER DATA BYTE, BIT #7	A	A
113	P1CA2	PARALLEL PORT 1, CA2 CONTROL LINE	(N/A)	B
114,115	GND	GROUND	-	-
116	P2CB1	PARALLEL PORT 2, CB1 CONTROL LINE	B	(N/A)
117	P1CA1	PARALLEL PORT 1, CA1 CONTROL LINE	B	(N/A)
118,119	GND	GROUND	-	-
120	P2CB2	PARALLEL PORT 2, CB2 CONTROL LINE	(N/A)	B

\*Signal categories are defined following this table.



TABLE 3 - (cont'd)  
SIGNAL CATEGORY DEFINITIONS

SIGNAL TYPE "A"			
INPUT		OUTPUT	
Max. Allowed Input Voltage	7.0V	Min. Guaranteed High Voltage	2.0V
Min. Allowed Input Voltage	0.0V	When Sourcing 14.6 mA	
Min. Allowed Input For "High"	2.0V	Max. Guaranteed Low Voltage	0.5V
Max. Allowed Input For "Low"	0.8V	When Sinking 23.8 mA	
Max. Current Sunked When Driven "High"	40 $\mu$ A		
Max. Current Sourced When Driven "Low"	220 $\mu$ A		

SIGNAL TYPE "B"			
INPUT		OUTPUT	
Max. Allowed Input Voltage	7.0V	Min. Guaranteed High Voltage	2.0V
Min. Allowed Input Voltage	0.0V	When Sourcing 15 mA	
Min. Allowed Input For "High"	2.0V	Max. Guaranteed Low Voltage	0.5V
Max. Allowed Input For "Low"	0.8V	When Sinking 24 mA	
Max. Current Sunked When Driven "High"	20 $\mu$ A		
Max. Current Sourced When Driven "Low"	690 $\mu$ A		

SIGNAL TYPE "C"		SIGNAL TYPE "D"	
INPUT		INPUT	
Max. Allowed Input Voltage	V <sub>cc</sub>	Max. Allowed Input Voltage	V <sub>cc</sub>
Min. Allowed Input Voltage	-0.3V	Min. Allowed Input Voltage	-0.3V
Min. Allowed Input For "High"	2.0V	Min. Allowed Input For "High"	2.0V
Max. Allowed Input For "Low"	0.8V	Max. Allowed Input For "Low"	0.8V
Max. Current Sunked When Driven "High"	2.5 $\mu$ A	Max. Current Sunked When Driven "High"	20 $\mu$ A
Max. Current Sourced When Driven "Low"	2.5 $\mu$ A	Max. Current Sourced When Driven "Low"	700 $\mu$ A



TABLE 3 - (cont'd)  
SIGNAL CATEGORY DEFINITIONS

SIGNAL TYPE "E" (RS-232C LEVELS)			
INPUT		OUTPUT	
Max. Allowed Input Voltage	30.0V	Min. Guaranteed High Voltage	7.0V
Min. Allowed Input Voltage	-30.0V	(Space) Across 3K Load	
Min. Allowed Input For "Space"	3.0V	Min. Guaranteed Low Voltage	-7.0V
Min. Allowed Input For "Mark"	-3.0V	(Mark) Across 3K Load	
Max. Current Sunked When	8.3mA		
"Space" (Von = 25V)			
Max. Current Sunked When	-8.3mA		
"Mark" (Voff = -25V)			

SIGNAL TYPE "F" (RS-422 LEVELS)			
INPUT		OUTPUT	
Max. Allowed Differential Voltage	±25v	Min. Guaranteed High Voltage When Sourcing 20mA	2.5V
Max. Allowed Common Mode Voltage	±15V		
Min. Differential Threshold Voltage (-7V ≤ VI ≤ 7V)	±0.2V	Max. Guaranteed Low Voltage Voltage When Sinking 48mA	0.5V
Max. Input Current:			
(A) For VI = 10V	3.25mA		
(B) For VI = -10V	3.25mA		



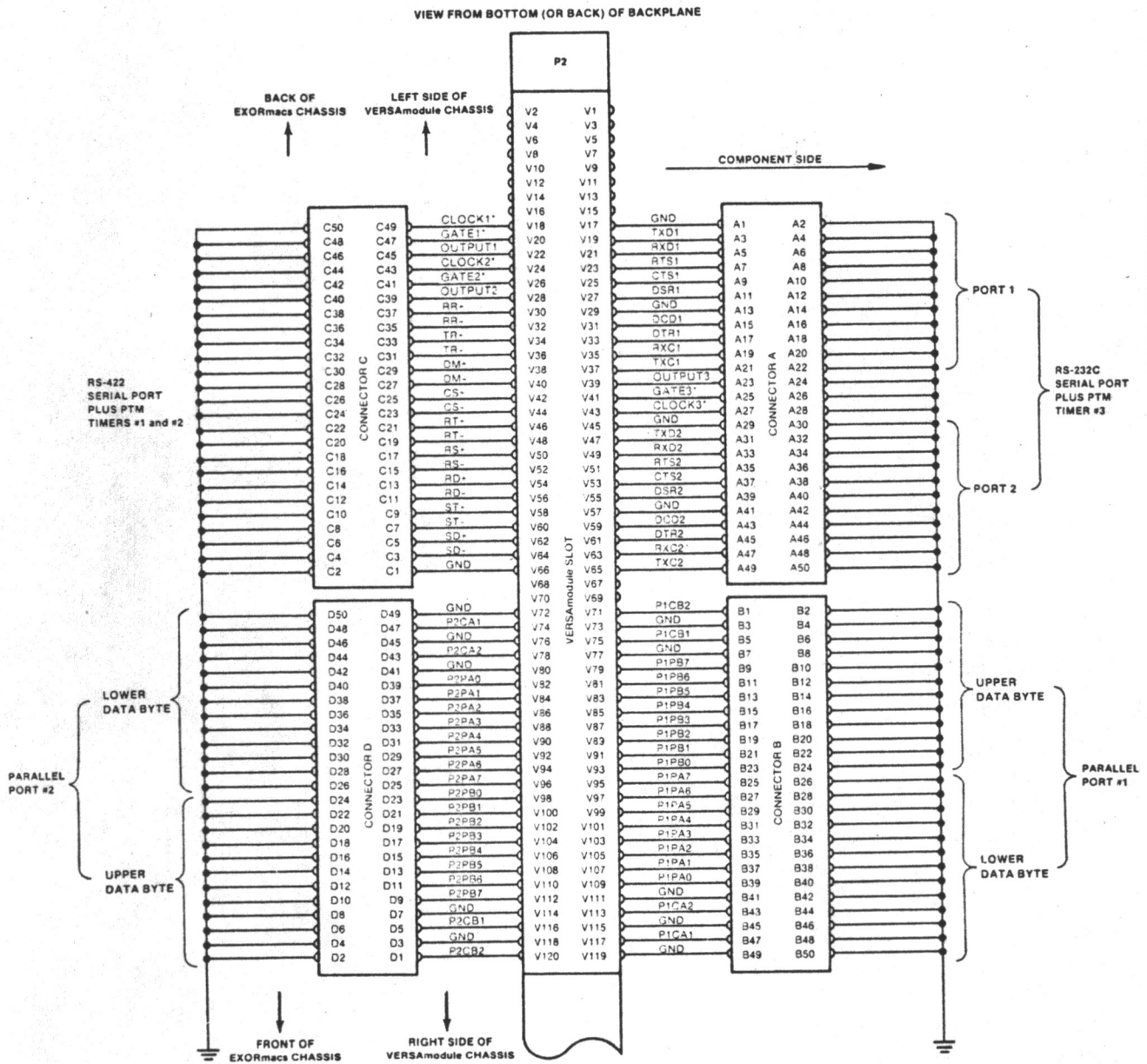
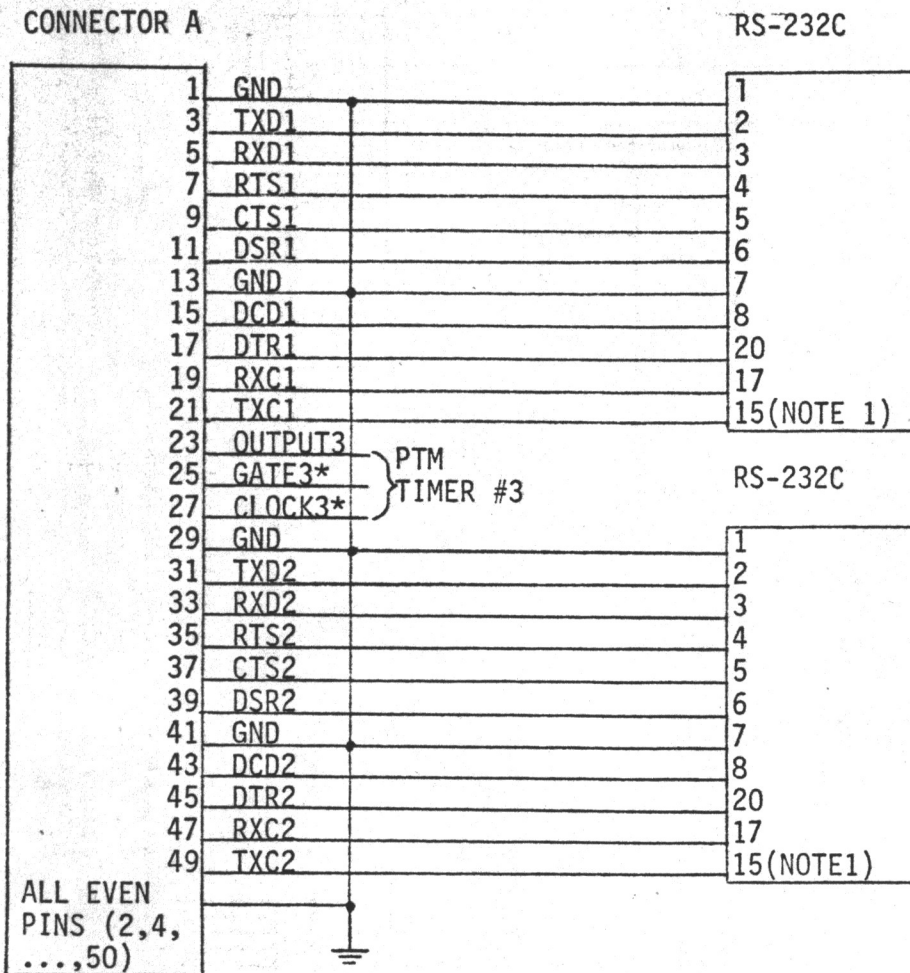


FIGURE 2-21. Peripheral Cable Connections to EXORmacs Chassis or to VERSAmodule Chassis (Sheet 1 of 2)





50-PIN CONNECTOR  
3M 3307-0000,  
AMP 88530-3,  
OR EQUIVALENT

USE RIBBON CABLE  
OR 26 AWG WIRE.

TWO 25-PIN CONNECTORS  
AMP 206646-1,  
3M 3482-1000,  
OR EQUIVALENT

#### NOTES:

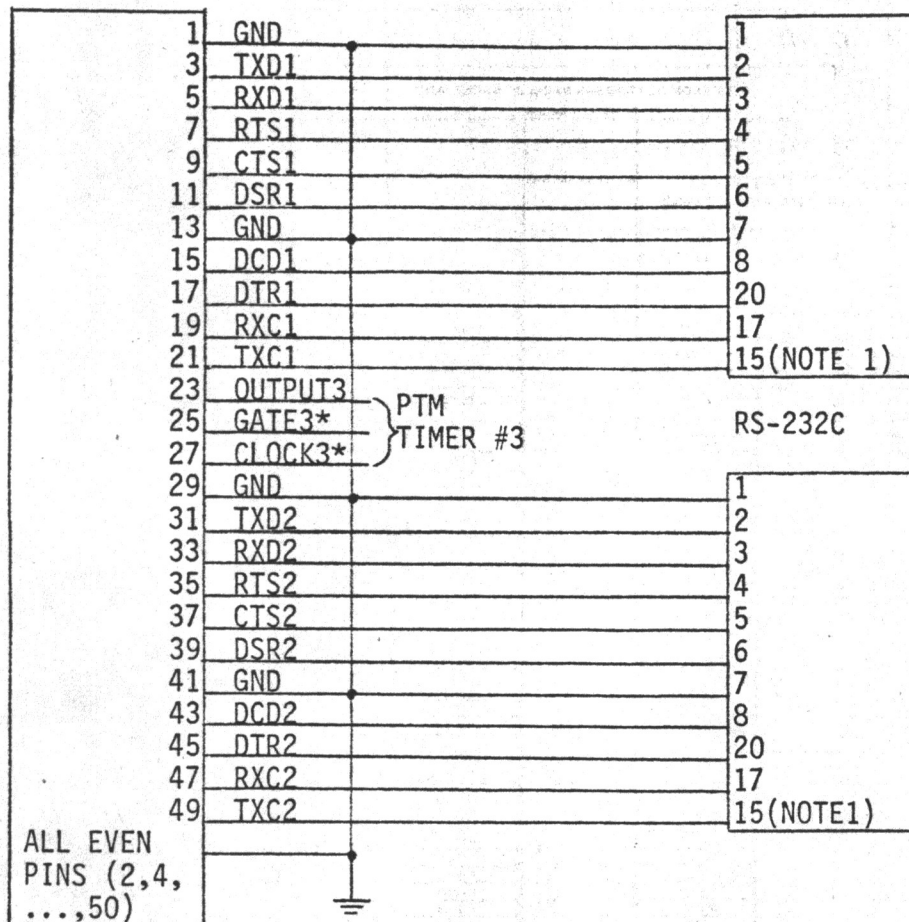
1. TXC SIGNAL IS ON PIN 15 WHEN THE MODEM IS SUPPLYING THE CLOCK. IF THE TERMINAL IS SUPPLYING THE CLOCK, TXC SIGNAL IS ON PIN 24.
2. ALL PINS NOT INDICATED ARE UNUSED AND SHOULD NOT BE CONNECTED.

FIGURE 2-21. Peripheral Cable Connections to EXORmacs Chassis or to VERSAmodule Chassis (Sheet 2 of 2)



CONNECTOR A

RS-232C



50-PIN CONNECTOR  
3M 3307-0000,  
AMP 88530-3,  
OR EQUIVALENT

USE RIBBON CABLE  
OR 26 AWG WIRE.

TWO 25-PIN CONNECTORS  
AMP 206646-1,  
3M 3482-1000,  
OR EQUIVALENT

NOTES:

1. TXC SIGNAL IS ON PIN 15 WHEN THE MODEM IS SUPPLYING THE CLOCK. IF THE TERMINAL IS SUPPLYING THE CLOCK, TXC SIGNAL IS ON PIN 24.
2. ALL PINS NOT INDICATED ARE UNUSED AND SHOULD NOT BE CONNECTED.

FIGURE 2-21. Peripheral Cable Connections to EXORmacs Chassis or to VERSAmodule Chassis (Sheet 2 of 2)



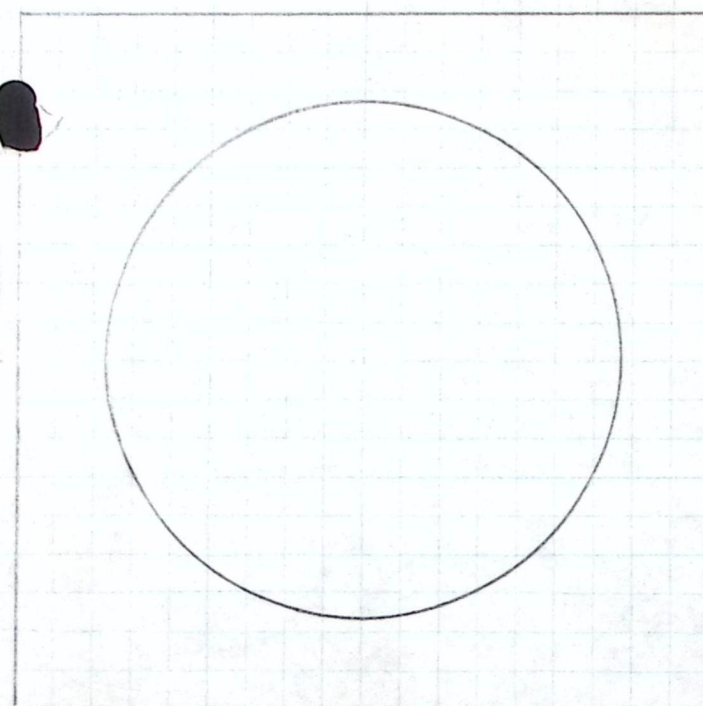
		Gray 1	Gray 2	Gray 3	Gray 4	
		Clip 1	Clip 2	Clip 3	Clip 4	Clip B
Depth pos.	Intensity pos.	Luminance 1	Luminance 2	Luminance 3	Luminance 4	Luminance B
Depth amp.	Intensity amp.	Start Blanking Field 1	End Blanking Field 1	Assign		
Depth Lock	Intensity Lock					

			CRT 1	CRT 2	CRT 3		
Segment 1	Segment 2	Segment 3	Segment 4	Segment 5	Segment 6	Segment 7	Segment 8

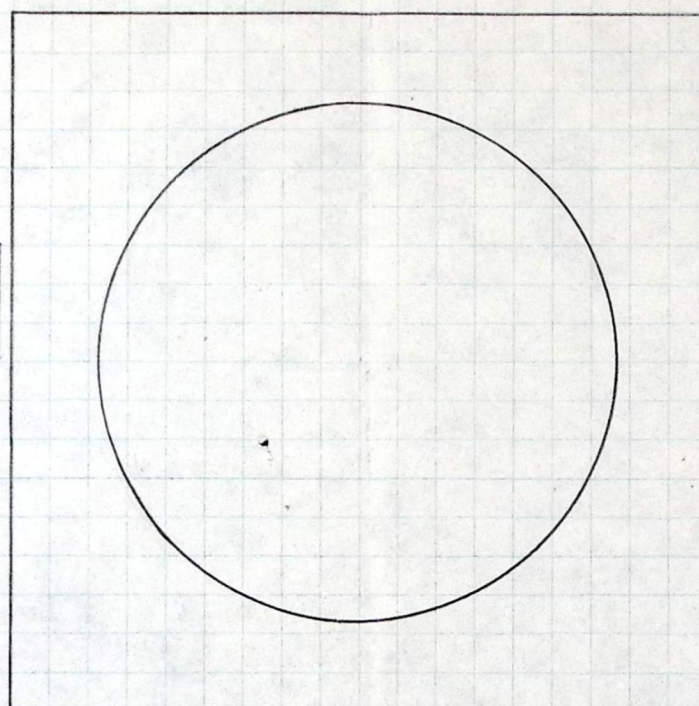
Length pos.	Width pos.	Red 1	Red 2	Red 3	Red 4	Red B
Length amp.	Length amp.	Start Blanking Field 2	End Blanking Field 2	Assign	Rotate X	
Length Lock	Width Lock					

Horz Axis pos.	Vert Axis pos.	Green 1	Green 2	Green 3	Green 4	Green B
Horz Axis amp.	Vert Axis amp.	Start Blanking Field 3	End Blanking Field 3	Assign	Rotate Y X-Y	
Horz Axis Lock	Vert Axis Lock					

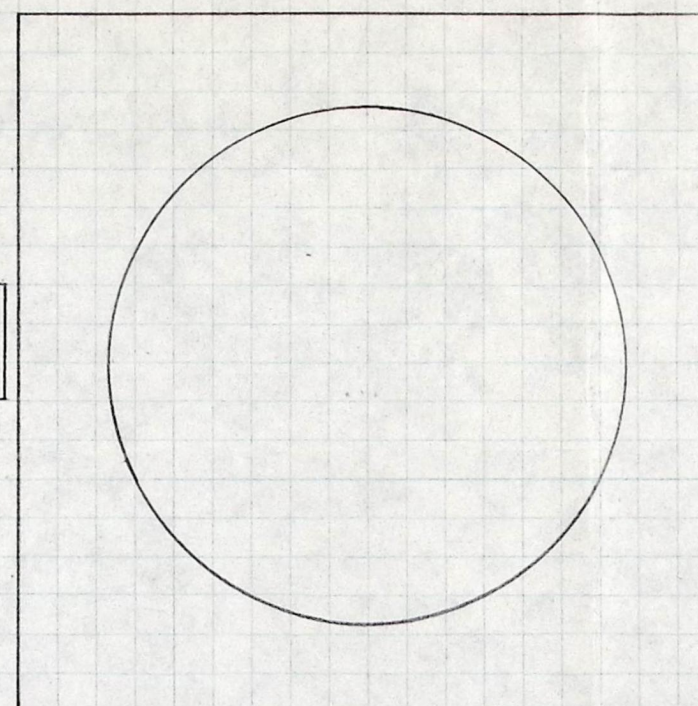
Horz Pos pos.	Vert Pos pos.	Blue 1	Blue 2	Blue 3	Blue 4	Blue B
Horz Pos amp.	Vert Pos amp.	Start Blanking Field 4	End Blanking Field 4	Assign	Rotate Z	
Horz Pos Lock	Vert Pos Lock					



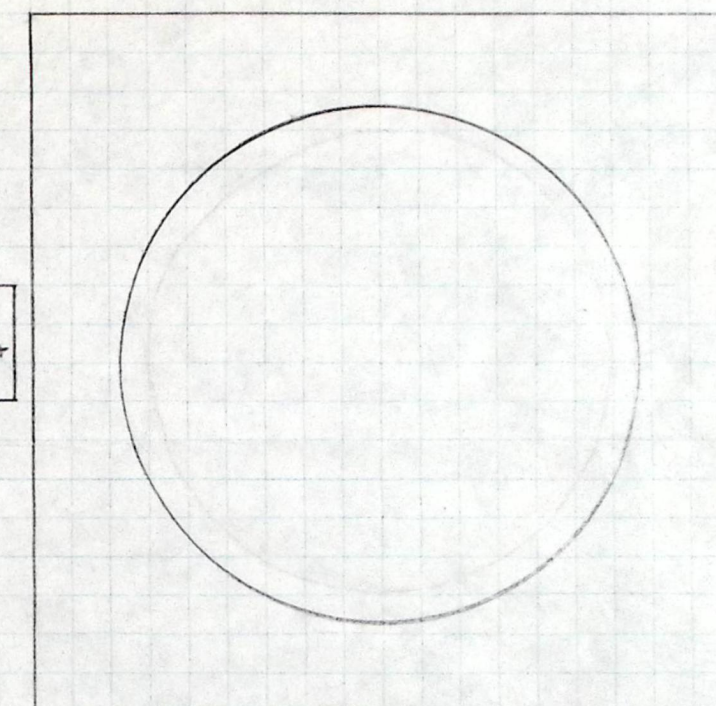
Course Adjust



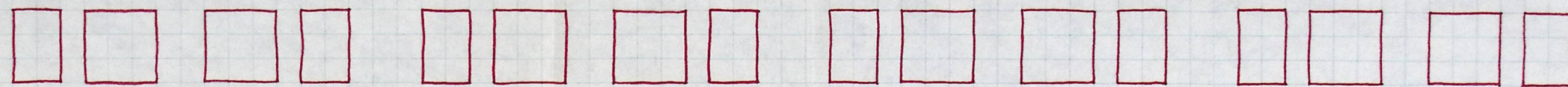
Course Adjust



Course Adjust





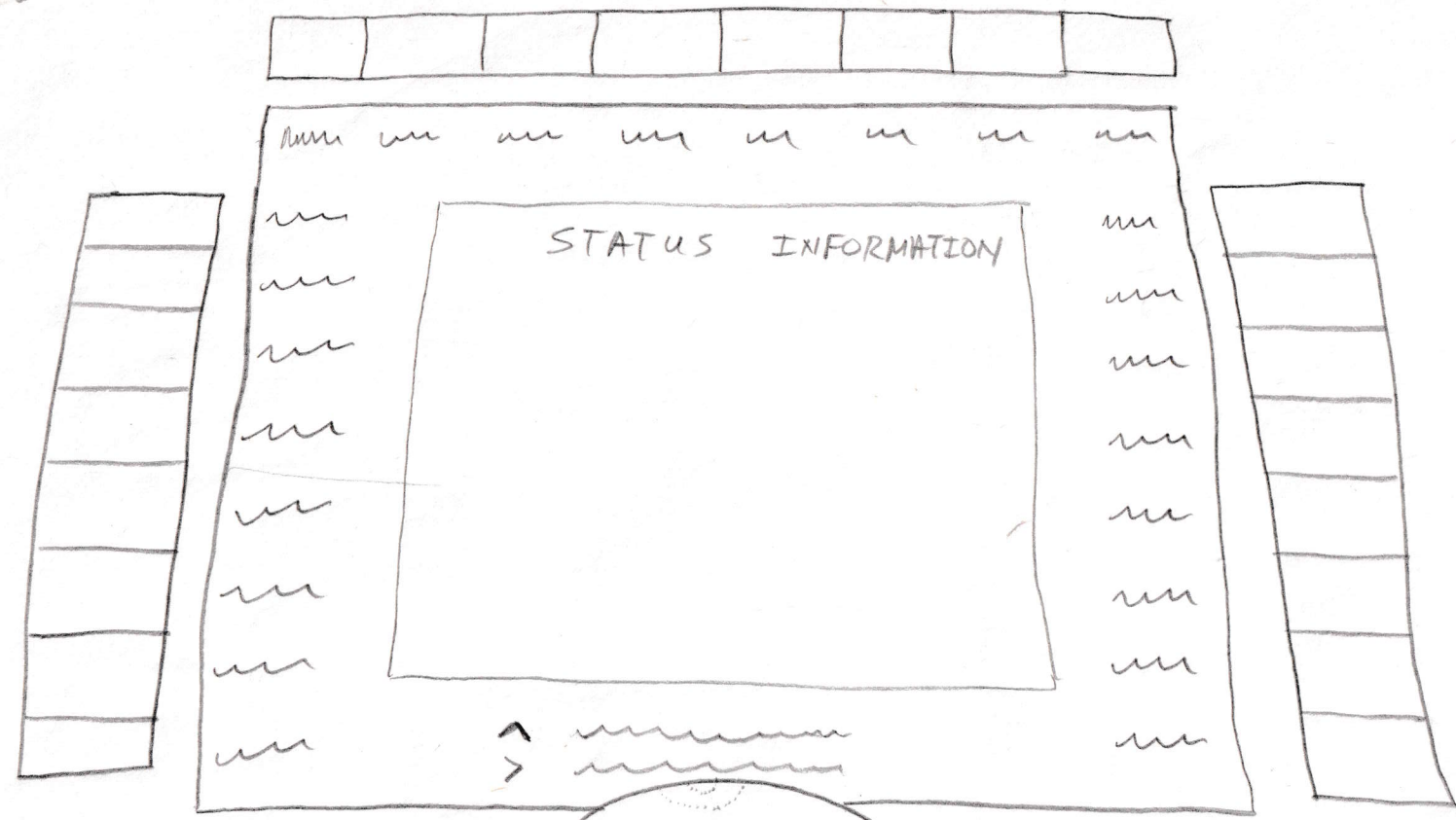




ONE OF FOUR  
PARAMETER  
CONTROL  
CLUSTERS

Double Key size, illuminatable  
Function keys labelled by CRT

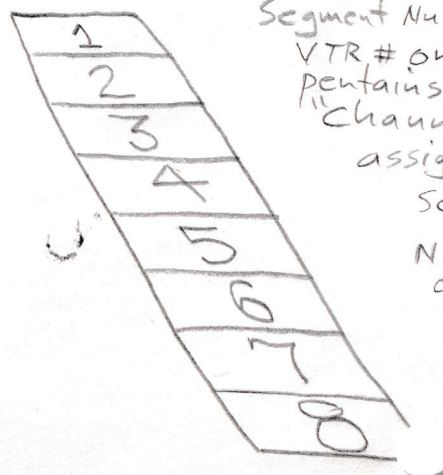
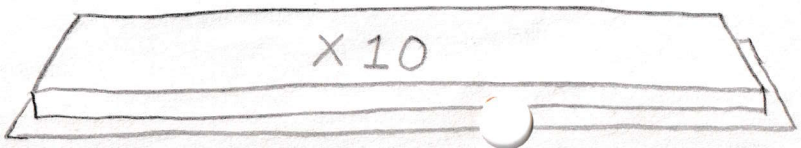
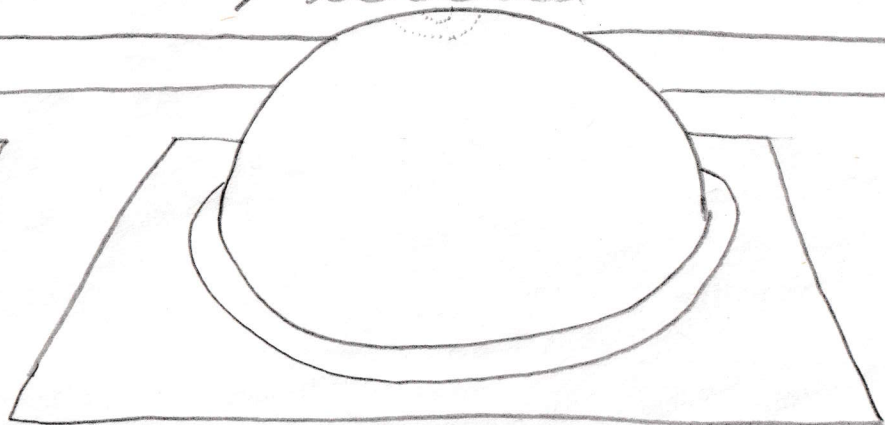
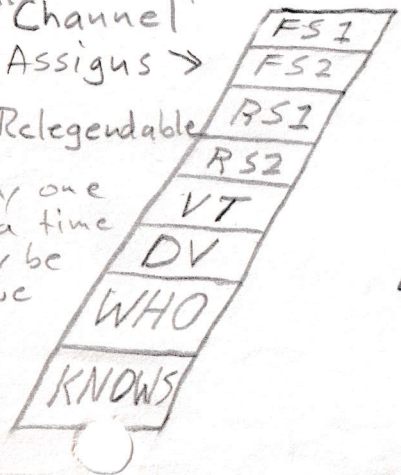
9" B+G mon @ 75°  
80 char by 24 lines



128  
functions

"Channel"  
Assigns →  
Relegendable

only one  
at a time  
may be  
active



Segment Number,  
VTR # on whatever  
pertains to  
"Channel"  
assignment  
selection.  
None, some  
or all may  
be active



19"

22.50

KB TB

Key'bd

JS TB KB JS

JS KB TB JS

450

350

350

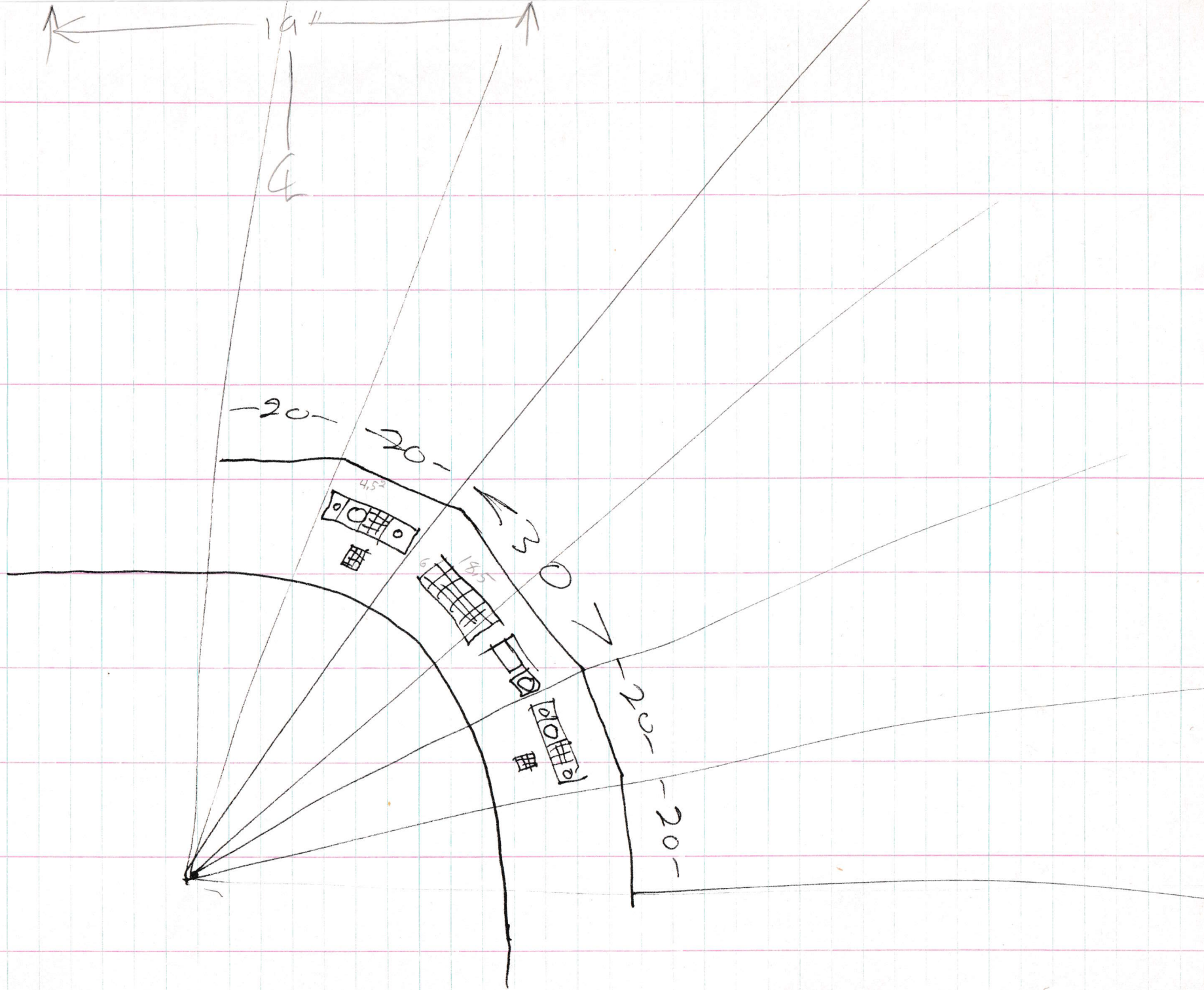
14" to Top

3' to ↑  
Moh

3' 8" ↑  
Center  
of Moh's

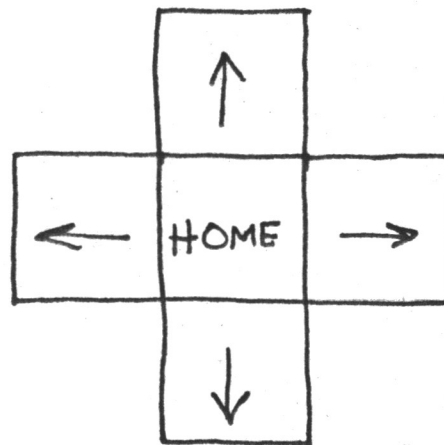






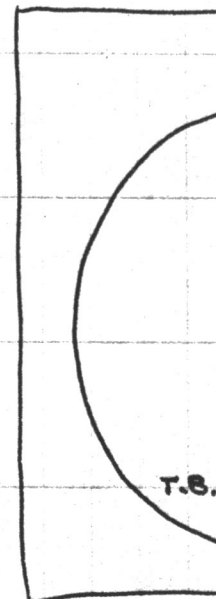


7	8	9
4	5	6
1	2	3
+	0	-
ENTER		:

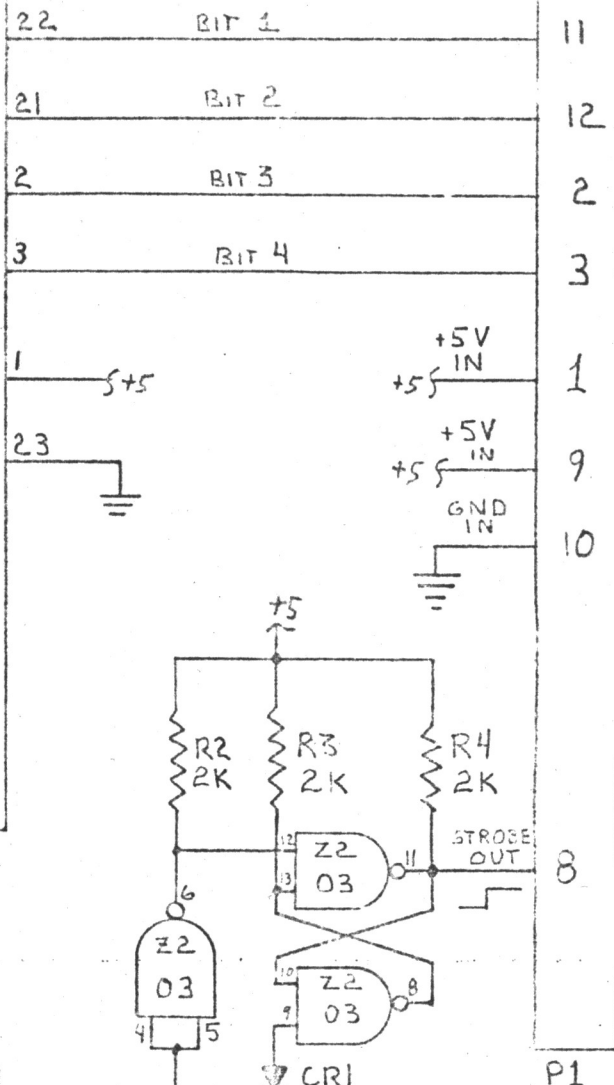
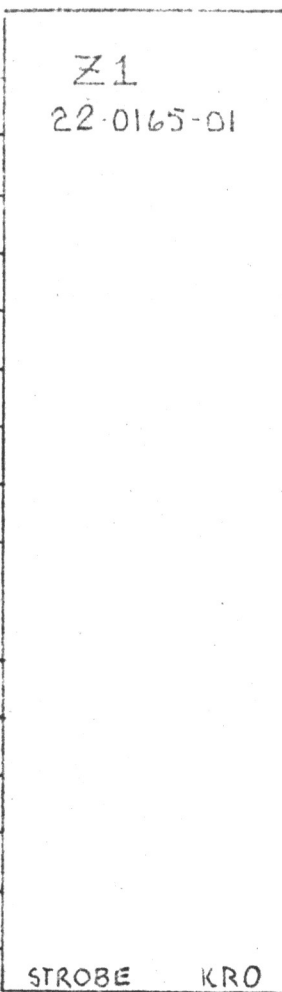
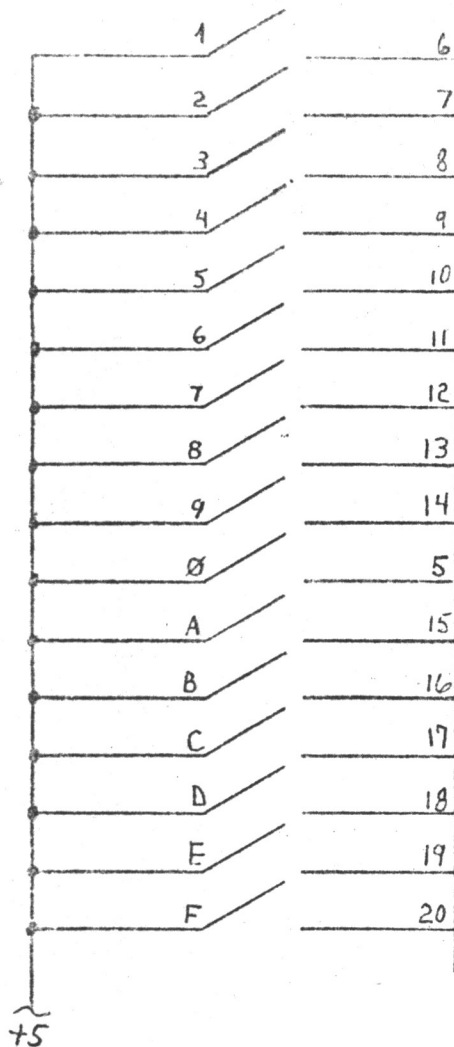


DELETE
ADD
REPLACE

LEFT HALF	BOTH <del>HALVES</del>	RIGHT HALF	
PLAY FROM LAST	PLAY THUR NEXT	PLAY LAST THUR NEXT	PLAY CURRENT







KEY	CODE
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A	1010
B	1011
C	1100
D	1101
E	1110
F	1111

1. SPEC NO. 36-0504

NOTES:

C	ECO# 5176 CORR. CIV. VALVE P/V	7/10/75
B	ADD SPECIFICATION NO. 65	7/9/75
REV.	DESC.	APP. DATE

SCALE

TITLE

16 KEY BCD ENCODED KEYBD.



**key tronic**  
**corporation**

SPOKANE, WASH. U.S.A.

DR. R. WENDER

DATE 10/24/71

APP.

DATE

DWG. NO.

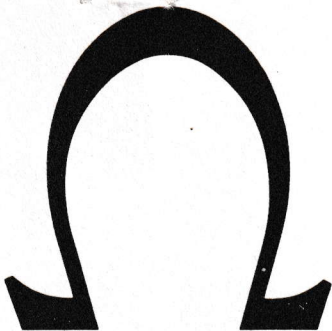
35-0504

SHEET

1 of 1

A (74)	CHG 20-0165-01 TO 22-0165-01 PER ECO 674	4/2/76	
REV.	DESCRIPTION	APP.	DATE





the total video systems company

**russ winselar**  
**vice president**

**omega video, inc.**  
14326 isis avenue  
lawndale, california 90260  
(213) 679-9021



# CHAR VIDEO

$$\text{ACTIVE HORIZ} = 1024 \text{ bits}$$

$$10 \text{ bit/char} = 102.4 \text{ char} - 102 \text{ chars}$$

$$\text{MAX CLOCK} = 3 \text{ MHz}$$

$$\text{ACTIVE VIDEO} = 34.133 \mu\text{sec} - 34 \mu\text{sec} (102 \text{ char})$$

$$\text{HORIZ blank} = 5.867 \mu\text{sec} - 6 \mu\text{sec} (10 \text{ char})$$

$$\text{Total line} = 40 \mu\text{sec} - 40 \mu\text{sec} 120 \text{ char}$$

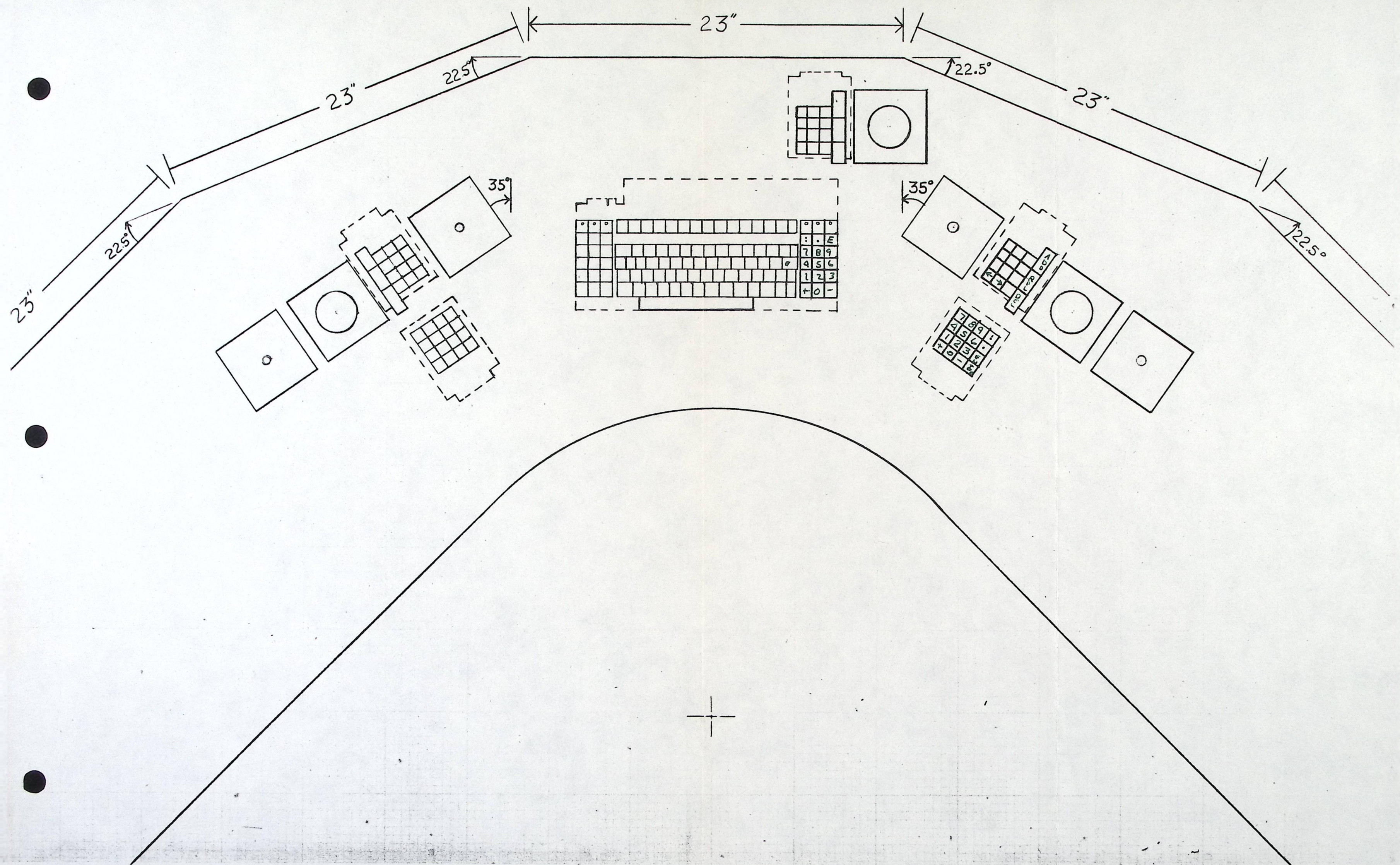
$$\text{Dot clock} = 30 \text{ MHz}$$

$$\text{HORIZ clock} = 25 \text{ KHz}$$

$$= 833.33 \text{ lines/frame}$$

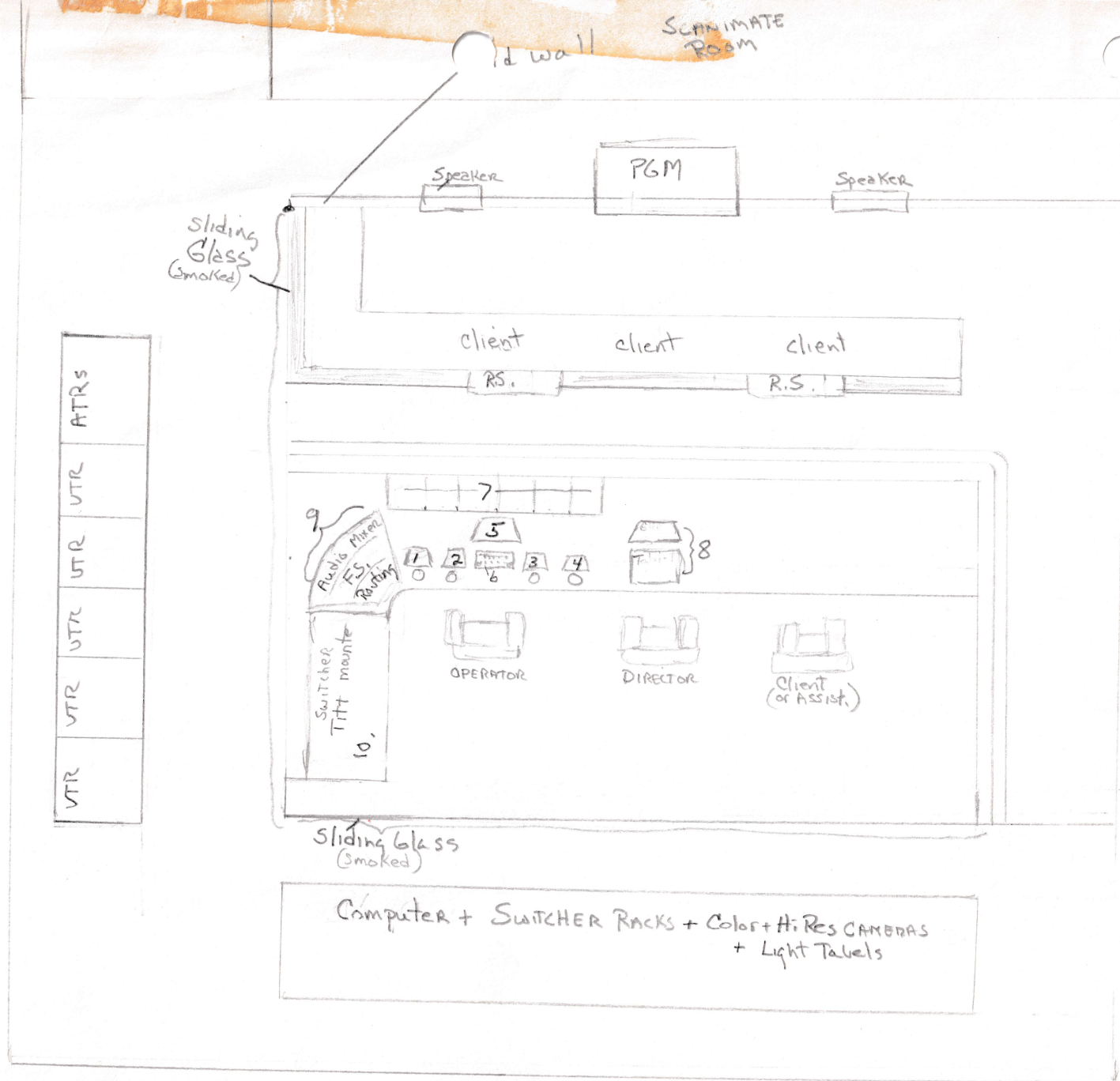
$$\begin{aligned} \text{want } 768 \text{ so } 833.33 - 768 &= 65.33 \text{ blanked} \\ &= 2.613 \text{ ms} \end{aligned}$$







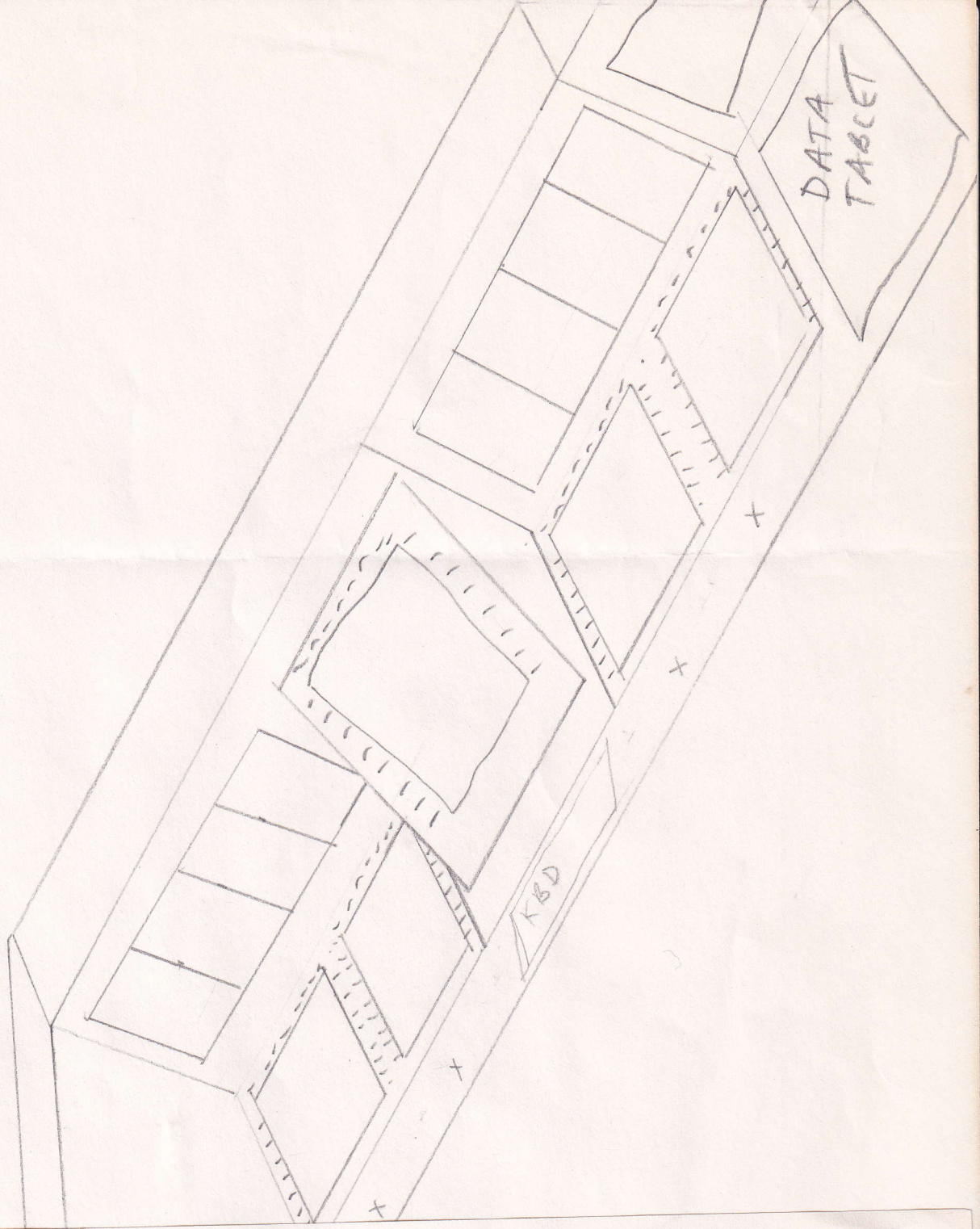
Peter's  
Dug



- 1-4 TRACKBALL + ASSOC. DATA MONITOR
- 5 - PRIMARY DATA MONITOR
- 6 - Keyboard
- 7 - Double Row of MONITORS CHNS. + VTRS + CAM.
- 8 - GRAPHICS TABLET + MONITOR

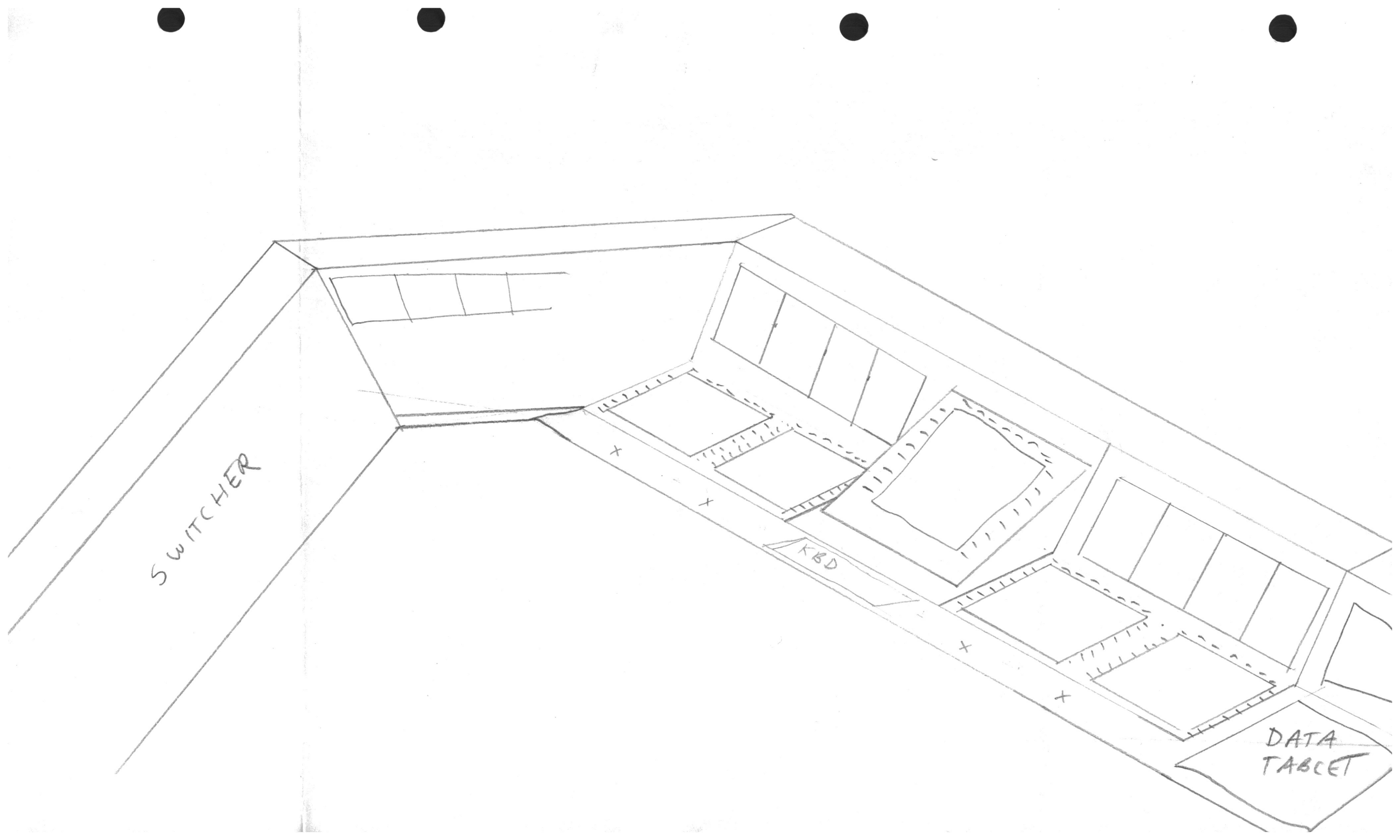
9. Audio Mixer + Audio control
- a) Routing to Video Monitors
- c) Frame Storer Remote control
10. Switcher (at tilt mount)





Roy's Dwg  
#1



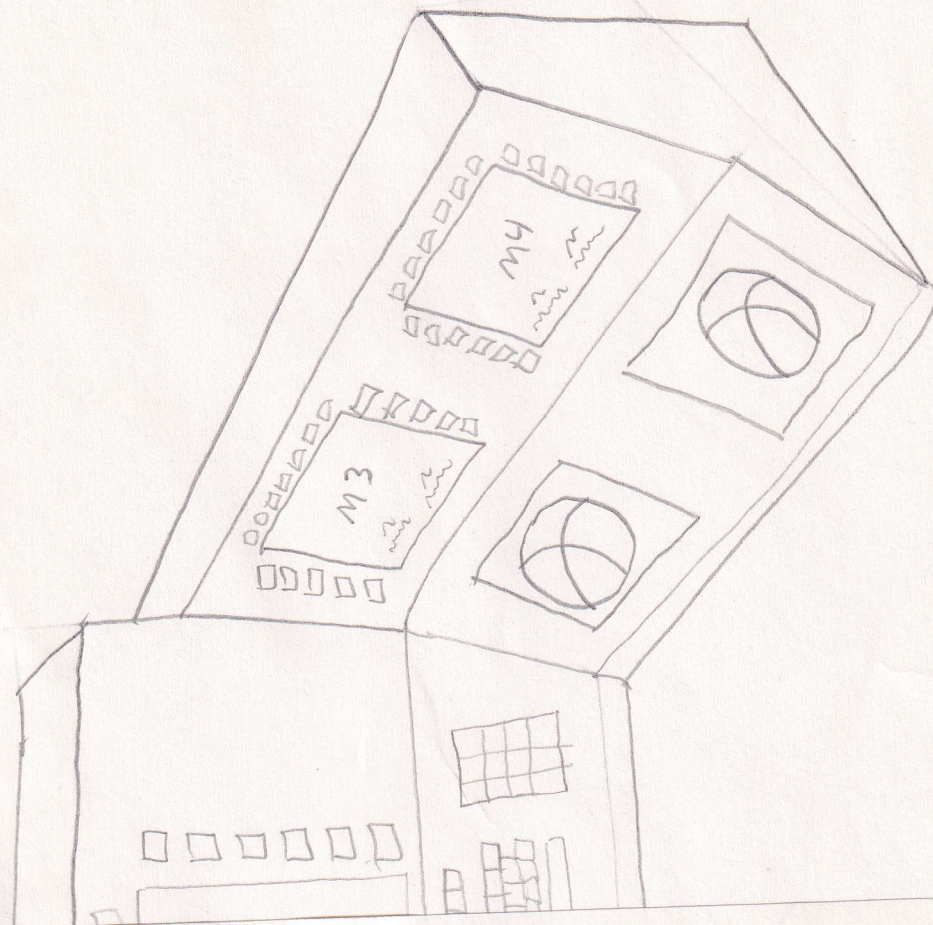


SWITCHER

KBD

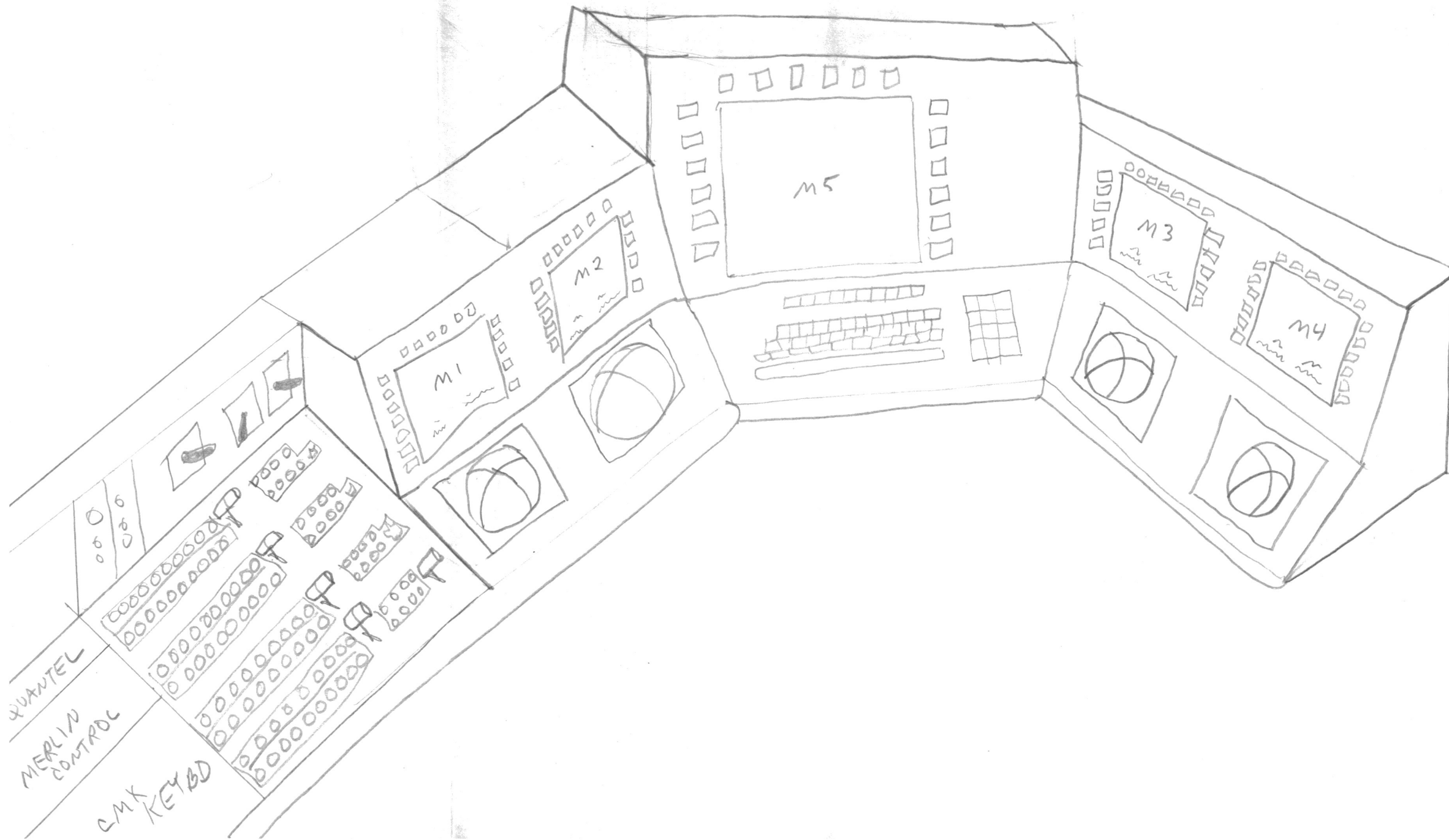
DATA  
TABLET



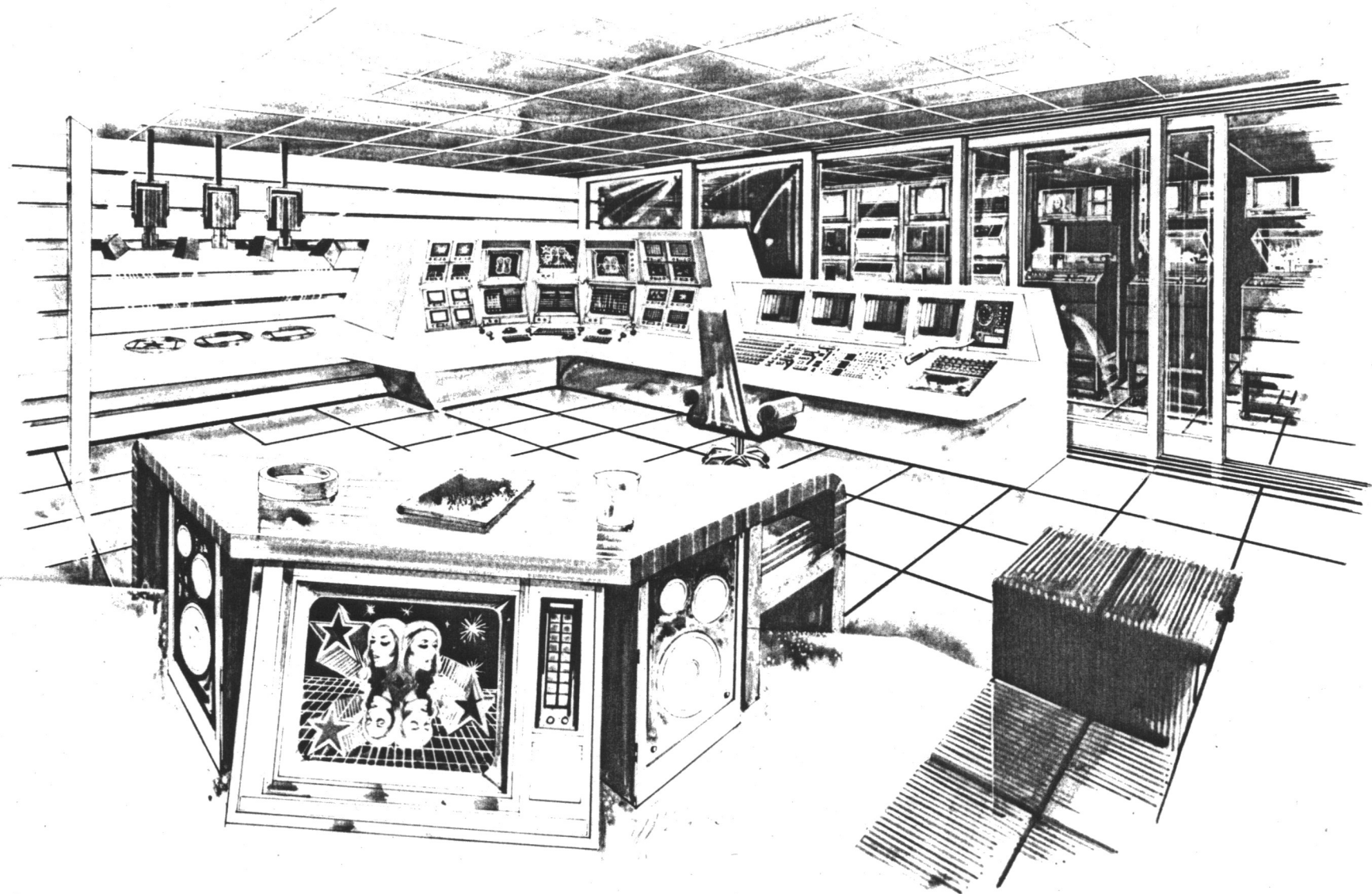


Roxs Dwg  
#2











PRELIMINARY

ANIMATION SCANNER PATENT:

**-SUMMARY-**

Disclosed is an electro-optical device for use in the creation of color television pictures making up an animated, or moving sequence from static photographic artwork. The basic principle involves the use of a cathode ray tube, also known as a C.R.T. upon which horizontal and vertical sawtooth voltages form a raster of scan lines. These lines are focussed upon a color photographic transparency, and the color and intensity of the light which is allowed to pass through is converted to voltages by photomultiplier tubes. These voltages then drive a color encoder which produces a color video signal in synchronism with the scanning raster on the C.R.T.

The unique approach taken by the inventors involves specific and precise control over many parameters which drastically affect the raster as it is drawn on the C.R.T. in real time. A digital computer is linked with a special purpose operator console, from which the operator may direct sequences of events, or change previously composed sequences to his liking. These sequences may be stored as digital information on a floppy disk. The digital computer is also connected to the following devices over which the operator has control via the computer: Waveform generators, which may be used to modulate any parameter; Video routing matrix, which may be used to connect various inputs and outputs in the system; Parameter controller, which provides a unique control function for each parameter of each segment; Timing generator, which controls the timing of each segment, or fraction of a frame; and Priority control, which may be used to assign levels of precedence for each segment as it occurs in real time.

Using these techniques, animations involving multiple layers of scenes, with complex movements, rotations, and perspectives may be produced from a single high quality color photographic transparency. Multiple digital computers may be linked on a common data bus, allowing control and storage of much more complex animated sequences.



PRELIMINARY

ANIMATION SCANNER PATENT:

**-DESCRIPTION OF THE INVENTION-**

Referring to **Figure #1**, the C.R.T. (4) is supplied with Vertical deflection voltages, (1) , Horizontal deflection voltages, (2) , and Re-trace blanking, (3). These form a standard television raster, timed to the applicable line and frame rate standards, (i.e. N.T.S.C, P.A.L, etc.). The raster is then directed optically in two directions by a partially reflecting mirror, (5). One portion of the light energy from the raster passes through the mirror, (5) and is focussed by lens (6) onto the photosensitive target of a Photomultiplier tube, (7). The resulting voltage is amplified by (8), resulting in an intensity compensation signal, (9) which shall be discussed later. The second path for light from the raster, results from its reflection off the front surface of mirror (5). This light energy is focussed by a lens (10), onto the emulsion side of a high quality color photographic transparency, (11). This transparency may be of any size. Light from the raster passes through the transparency, and is modulated both in intensity and in color. A lens (12) focusses the light into photomultipliers (14, 18, 21) via dichroic mirrors, (13, 17). The first mirror, (13) causes red light to be reflected into the red Photomultiplier, (14), while allowing blue and green light to pass through. The next mirror, (17) causes blue light to pass through to the blue photomultiplier, (18), while allowing only green light to pass through to the green photomultiplier, (21). Each photomultiplier converts the instantaneous light level incident upon it into a corresponding voltage, amplified by (15, 19, 22), resulting in red, green, and blue video voltages. (20, 23, 16). Power supply (25) provides the four photomultipliers with high voltage of a negative polarity, (24).



PRELIMINARY

ANIMATION SCANNER PATENT:

**-DESCRIPTION OF THE INVENTION-**

Referring to **Figure #2**, a Digital Computer,(26) is connected to peripherals and other computers via bi-directional bus,(27). Connection is made to a digital disk storage unit,(29), a specialized operator console,(30), a video routing matrix,(31), and to other similar animation systems at (28). Unidirectional bus connections are made to sixteen analog waveform generators,(32) whose outputs form an analog bus (39). Unidirectional bus connections are also made to the parameter controllers,(33), timing generator(34) and to the priority control,(35). The priority control determines the priorities of eight external signals, representing video matte shapes,(36), and outputs a digital number corresponding to the highest priority signal present at any given time (37). Assignments of priority levels to the various matte shape inputs is under control of the digital computer,(26). The timing generator,(34) compares the priority information,(37) with the synchronization signals (41) under control of the digital computer,(26), resulting in segment logic signals,(38) which gate the proper parameter data into the parameter controller,(33). The parameter controller's primary function is to provide the proper control signals to the raster generator,(40), the three dimensional rotation controller,(49), and the color controller,(46), on a segment by segment basis. The digital computer,(26) loads data into the parameter controller during the vertical retrace period of each frame. The parameters controlled in this manner are: X size, X axis, X position, Y size, Y axis, Y position, Z size, Z axis, Depth, Focal length, R,G,and B White level, and R,G,and B black level. Referring to **Figure #3**, it can be seen that data from the digital computer,(27) is stored in a memory block,(53), which is organized as eight words of twelve bits each. The segment information, (38), gates one of the words to the digital to analog converter,(54,) where it is converted to a corresponding analog voltage. The same process takes place in memory blocks,(56, 59) which drive digital to analog converter (57) and an analog switch (60),respectively. The second converter,(57) is used with multiplication element,(58) to affect the amplitude and polarity of the analog signal selected by the switch,(60). The analog signals selected by the switch,(39) originate in the waveform generators.(32). The outputs of the first digital to analog converter,(54), and the multiplier,(58) are summed by the addition element,(55) and result in one of the sixteen parameter outputs.(61)



PRELIMINARY

ANIMATION SCANNER PATENT:

**-DESCRIPTION OF THE INVENTION-**

Referring to **Figure #4**, details of the Raster generator can be seen. Horizontal synchronizing pulse,(62) enters ramp generator,(63), resulting in a linear sawtooth voltage entering multiplication element,(64). The Y size parameter output,(67) is the multiplicand for elements,(64, 65). The second input for multiplier,(65) is the parameter controller Y axis output,(68). The results of these two operations are summed at additive element,(66) to produce the Y output (69), for driving the three dimensional rotation unit. A similar operation takes place in the vertical portion of the raster generator. Referring to **Figure #4**, it can be seen that vertical synchronizing pulses,(70) enter ramp generator,(71), resulting in a linear sawtooth voltage entering multiplication element,(72). The X size parameter output,(75), is the multiplicand for elements,(72, 73) The second input for multiplier,(73) is the parameter controller X axis output,(76). The results of these two operations are summed at additive element,(74) to produce the X output,(77) for driving the three dimensional rotation unit.

Referring to **Figure #5**, it can be seen that a basic two dimensional rotation unit is disclosed. An X input,(78) and a Y input,(79) are provided to multipliers,(82, 83, 84, 85). The multiplicands to these elements are generated by sine and cosine functions of digital word N, at (80) in item,(81). The outputs of summing elements (86, 87) are the original X and Y rotated by the digital angle N. The items disclosed in **Figure #5** are drawn in simplified form in **Figure #6** as a single element,(90, 91, 92, 104). The rotated signals at (88, 89) are applied to rotation units,(91, 92), as well as the Z parameter output,(95). Thus, changing the digital angle,(93) causes the raster to rotate about it's X axis, and changing the digital angle,(94) causes the raster to rotate about it's Y axis. The Depth input,(96) affects the size of the raster, while the Focal length input,(101) affects the perspective of the raster, thus simulating the optical characteristics of a wide angle or telephoto lens. Rotation element,(104) rotates the final image through a digital angle,(105), and the outputs are summed with positional parameters,(108, 109) in elements(106,107) to provide X and Y outputs to the C.R.T, (110,111)



PRELIMINARY

ANIMATION SCANNER PATENT:

**-DESCRIPTION OF THE INVENTION-**

As can be seen from Figure #7, by way of example, a photographic transparency is shown in (a) upon which an exposure has been made of the alphabet. While this would normally be done in color, we shall presume for sake of illustration that this is black and white, and that we can see the position of the scanning raster behind the film. Notice that in (a) only the upper right-hand quarter of the film is being scanned. However; the full raster is scanning this area, thus, the output screen at (b) contains what appears to be a blowup of one quarter of the film. In fact by reducing the size of the raster even further, so that the full frame of raster appears behind only the letter "Q", That letter may be made to fill the output screen. Notice that the only factors affecting the resolution of the image on the output screen are the quality of the film transparency, and the scanning standards in use.

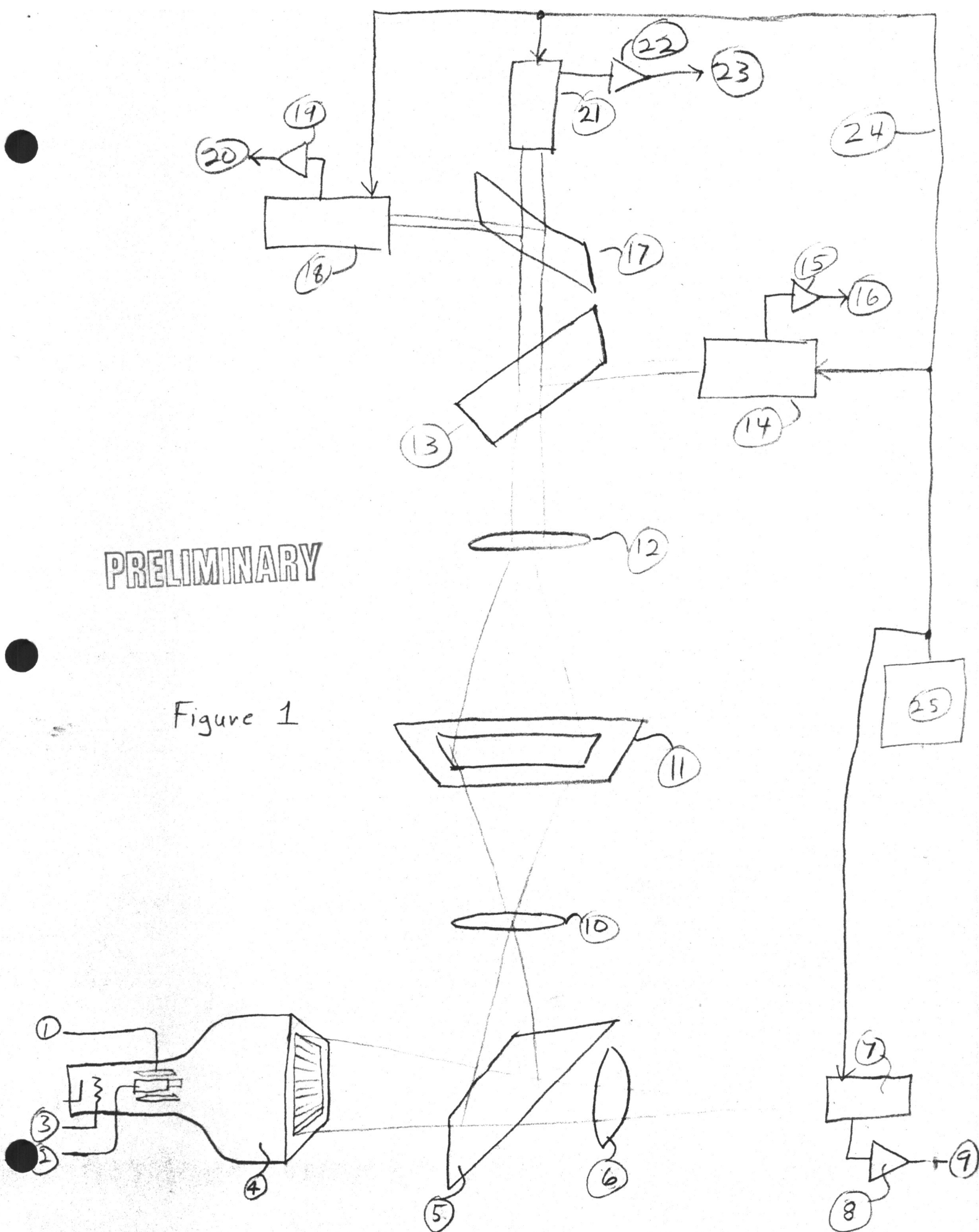
In the figure at (d), the raster has been rotated in a counter-clockwise direction, resulting in the clockwise rotation observed at (e). The raster may be sized and rotated in any manner, such as at (f). Unique effects may be observed at the output screen, if rotations about the X axis, (g & h); or Y axis, (i); are performed.

All of the above presume only one segment. However; if multiple segments are used, effects such as those in (k) may be produced. The majority of the frame, the raster scans in the football shape centered around the letter "Q". This shape is caused by one of the waveform generators affecting X size. This results in the curved appearance of the letters "P,Q,&R" on the output screen. The star shape is an external matte signal fed to the priority unit, causing the segment to switch to new parameters during the time the star shape is valid. Thus, by changing that segment's position parameters, any letter could be made to appear inside the star shape. The letter "I" is another segment caused by an external matte signal. That segment's raster has been rotated about the X axis to cause the perspective shown in (k). Since control of all the above elements is handled by a digital computer, each parameter can change on a frame by frame basis, thus resulting in animation. More examples of segmented operation are shown in figures (l, m).



PRELIMINARY

Figure 1





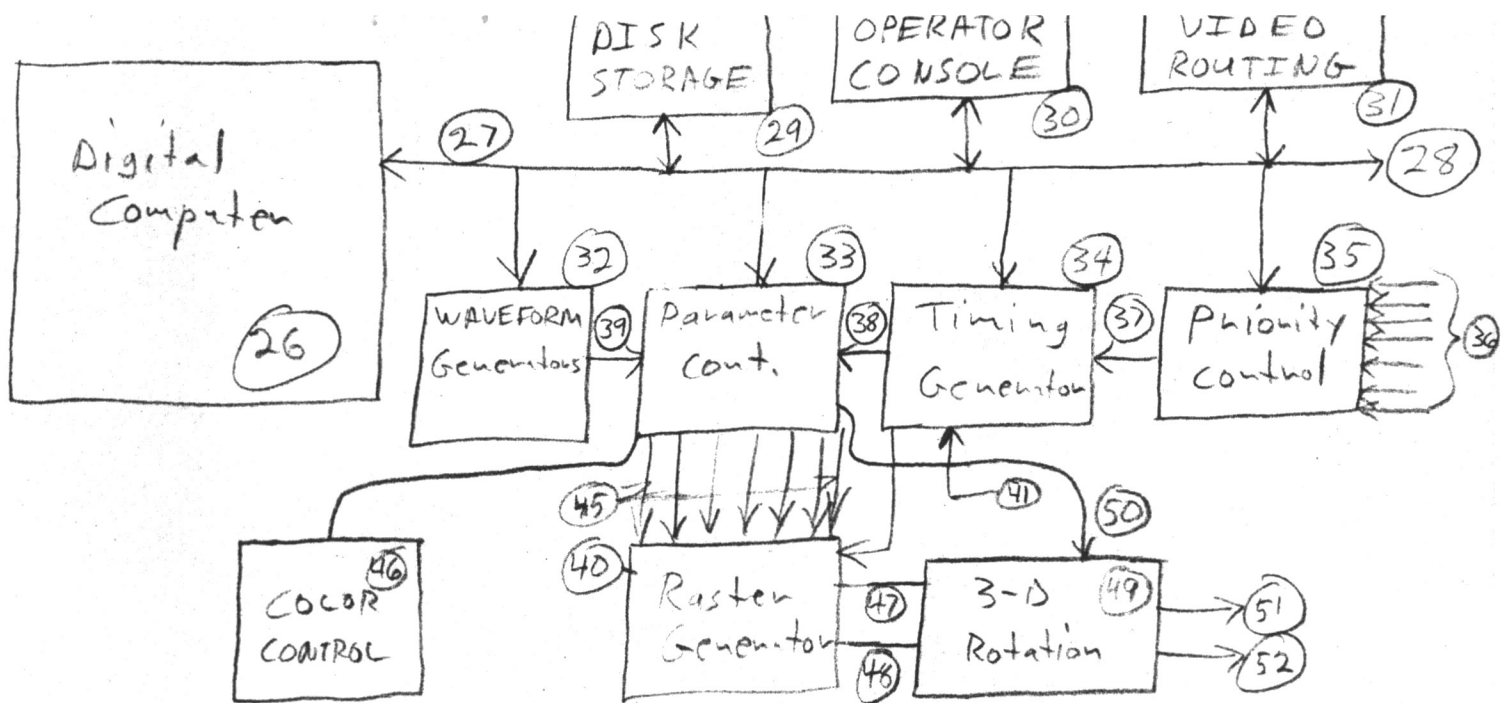


Figure 2

PRELIMINARY

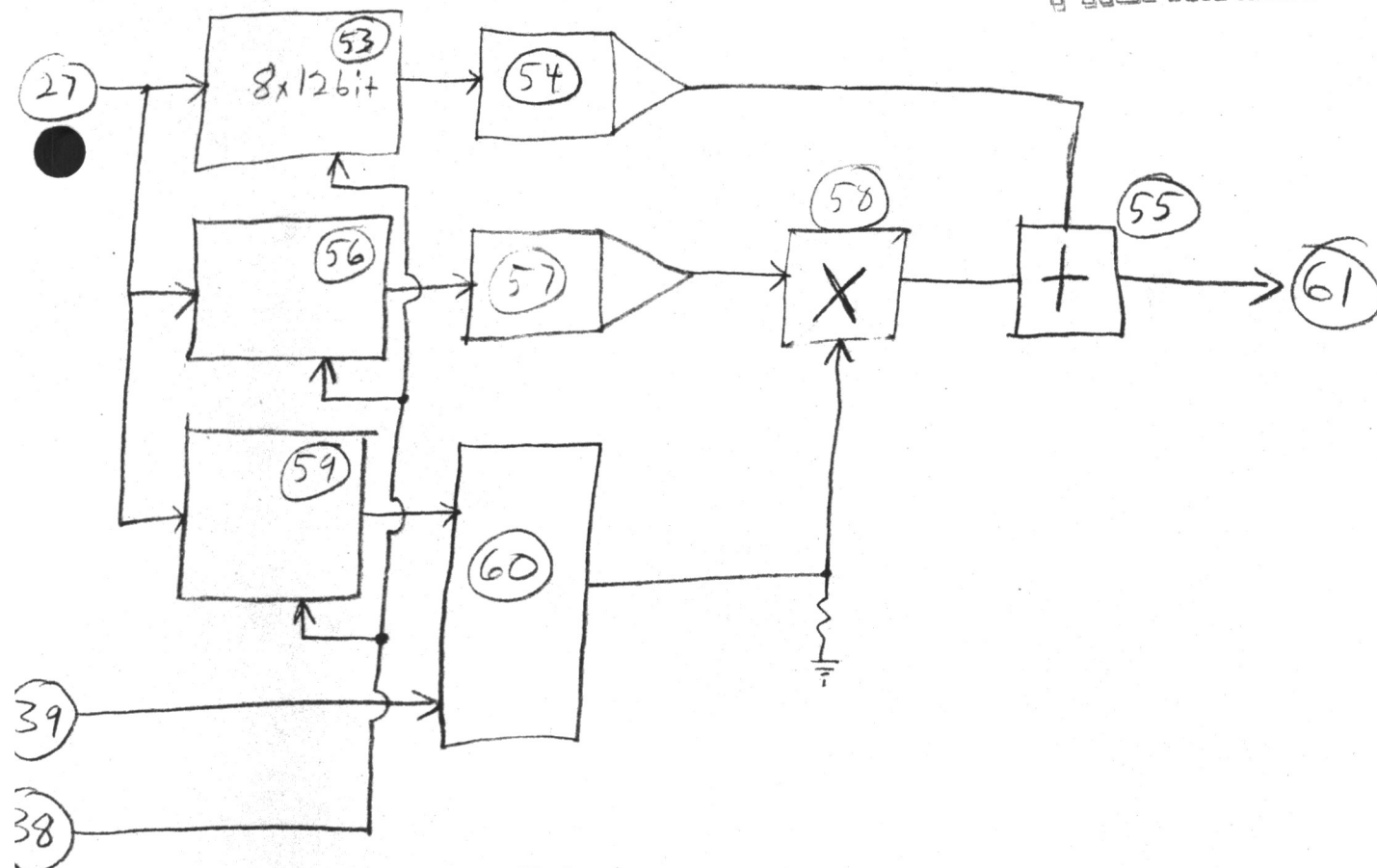


Figure 3



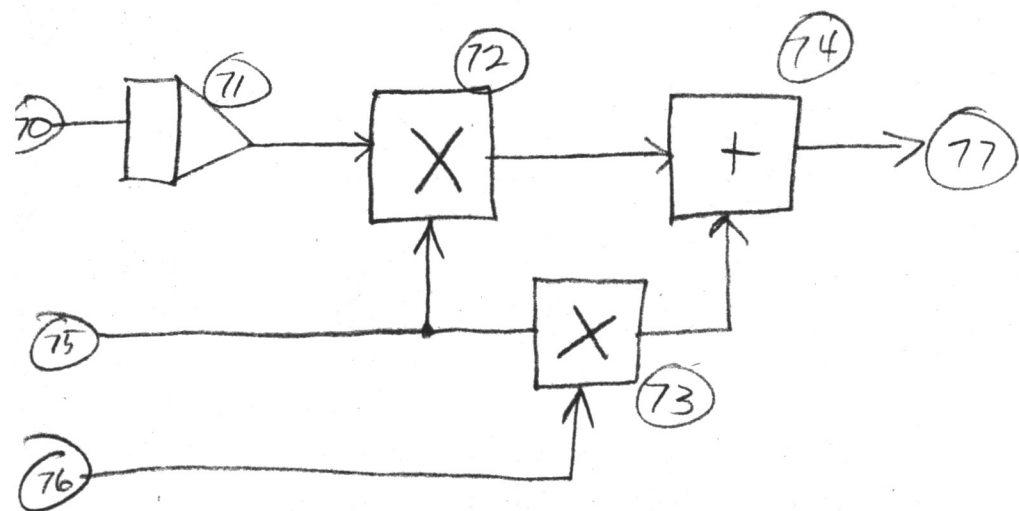
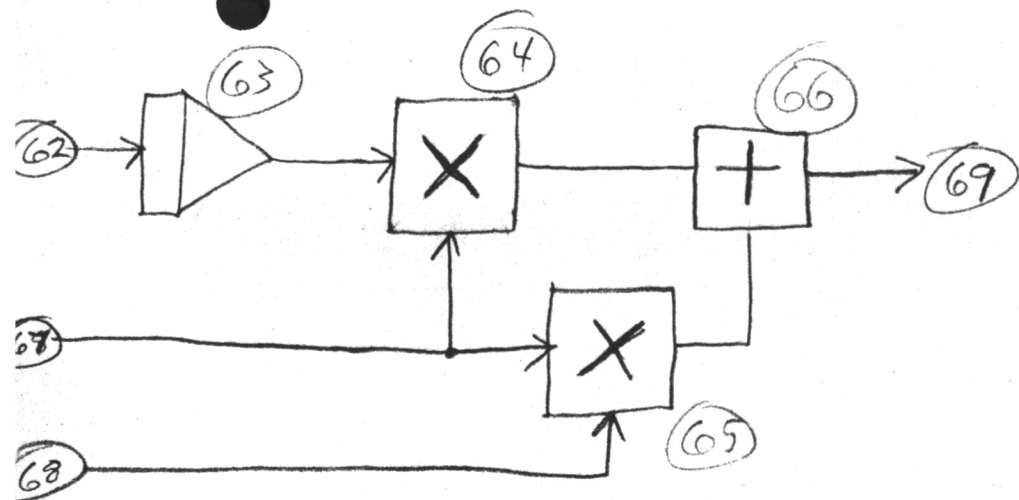


Figure 4

PRELIMINARY

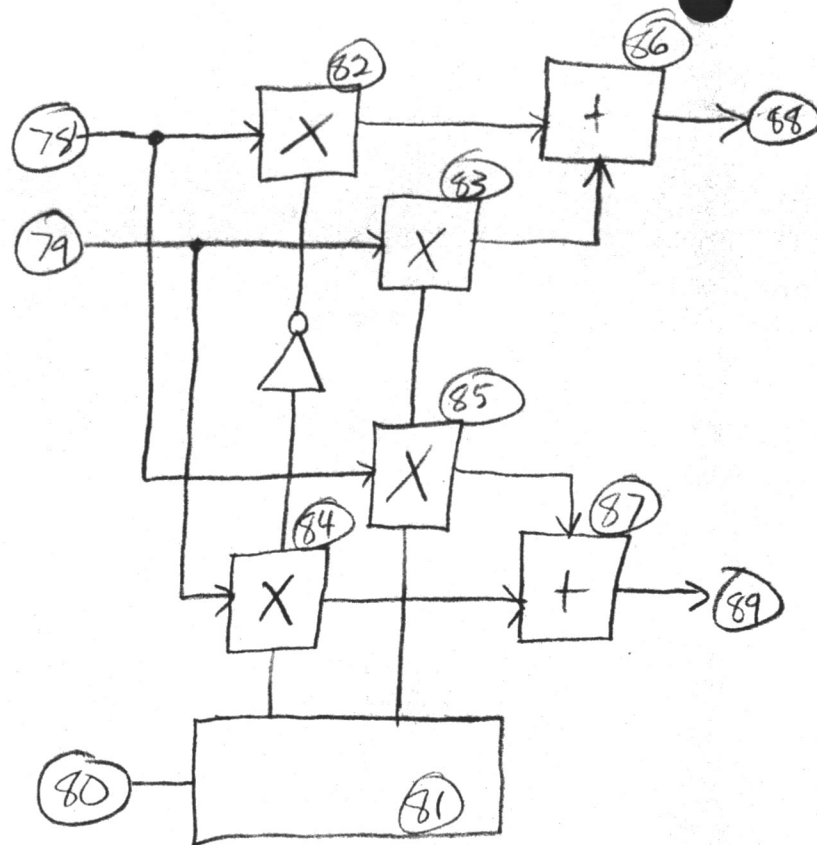


Figure 5



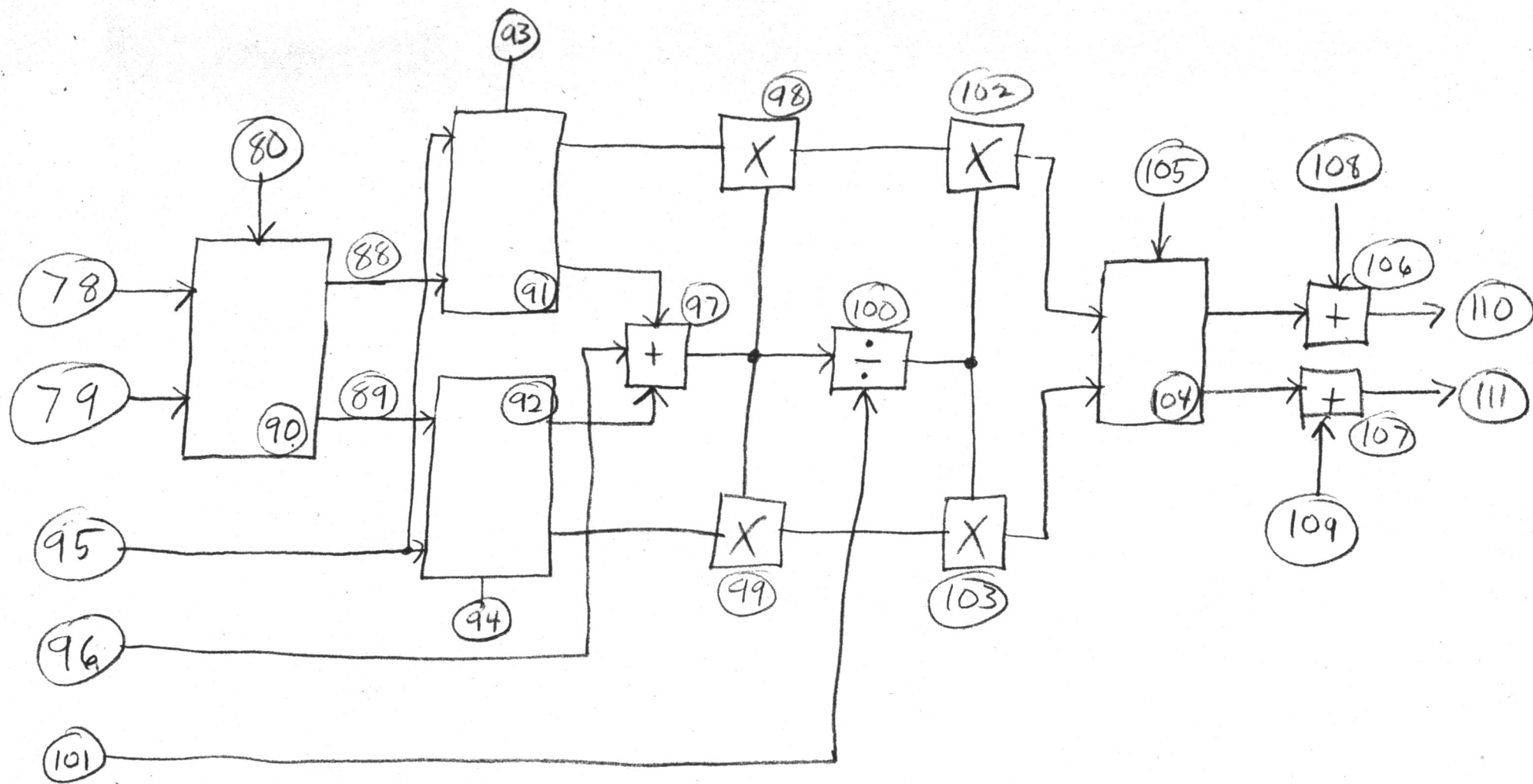


Figure 6

PRELIMINARY



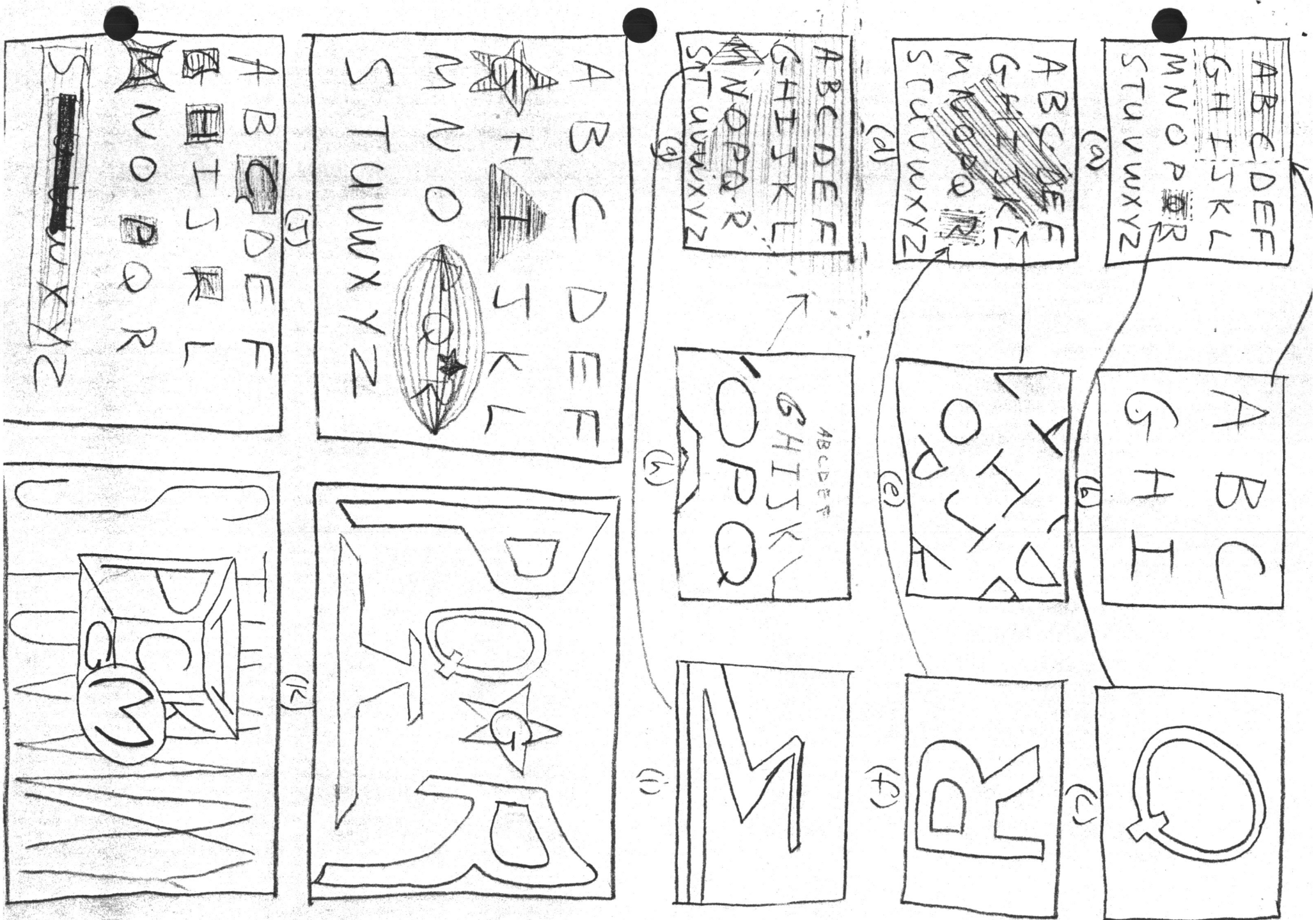
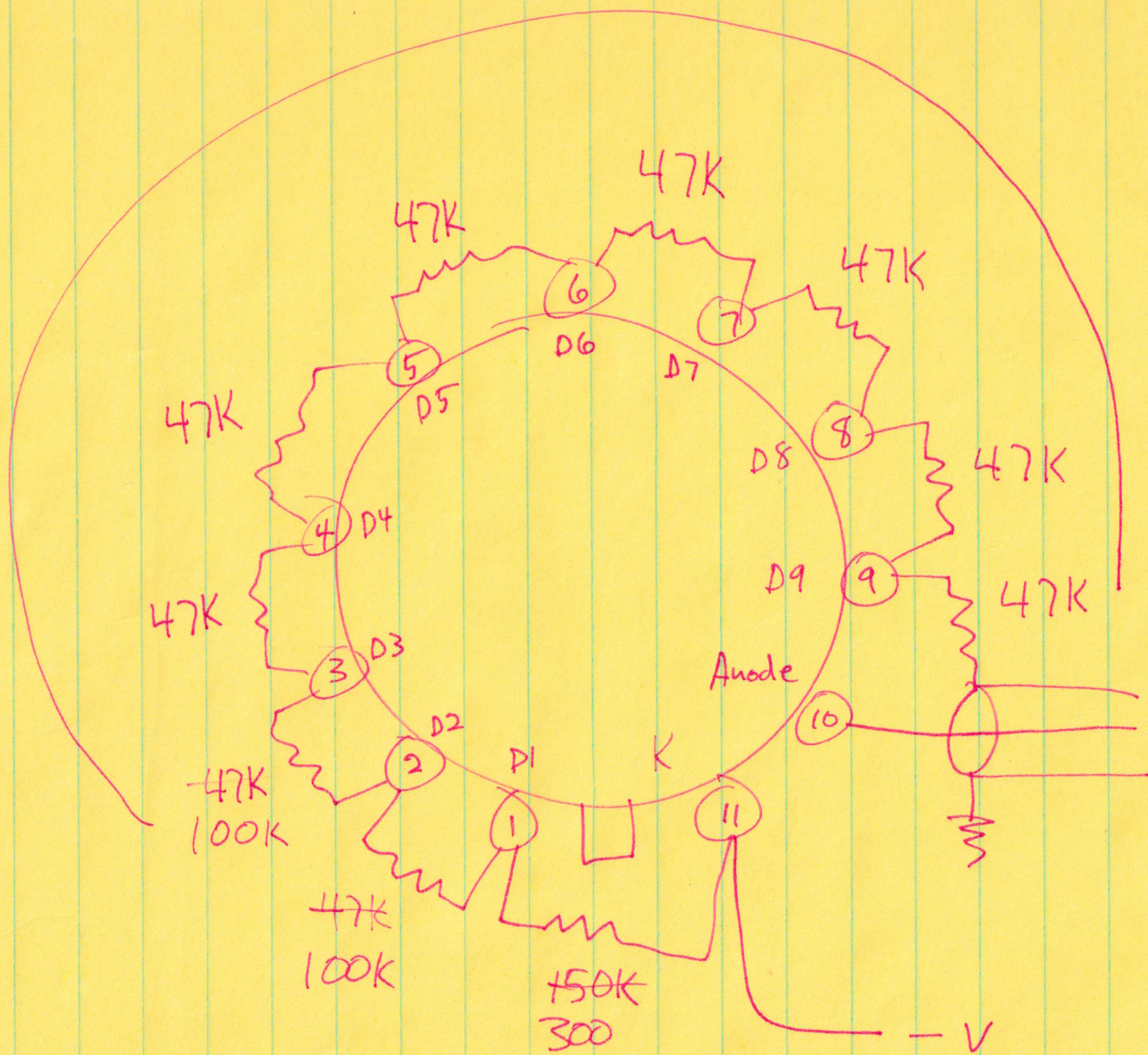


Figure 7

PRELIMINARY





AM



880

1244 V peak

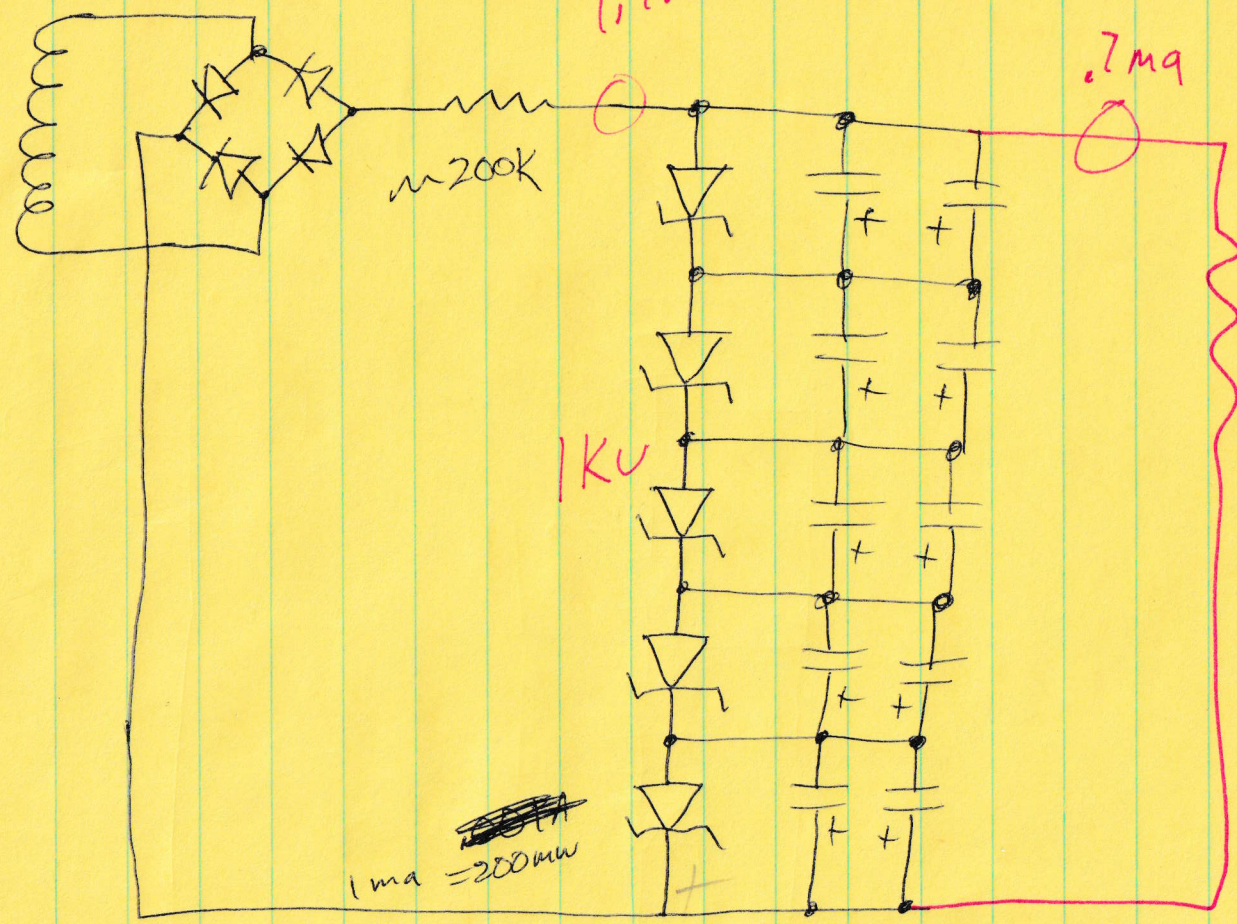
1.7 mA

.7 mA

1.3 MΩ

1 KΩ

~~100 mA~~  
1 mA = 200 mW



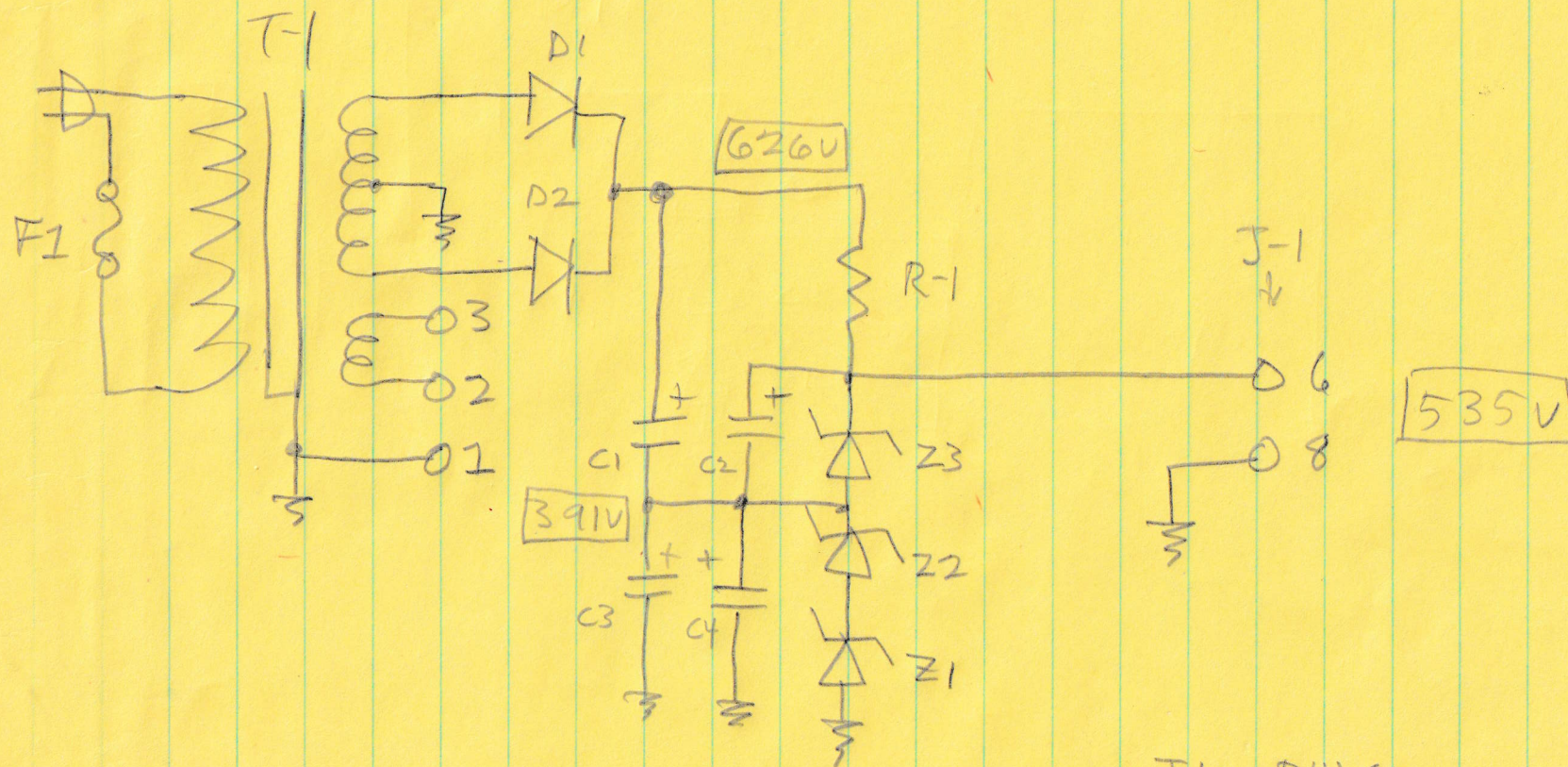
1100 V

PMT

REG



Jeanne McConnel  
 VIP  
 485-0866



Vacuum Tube Power Supply  
 5-22-81 DWS

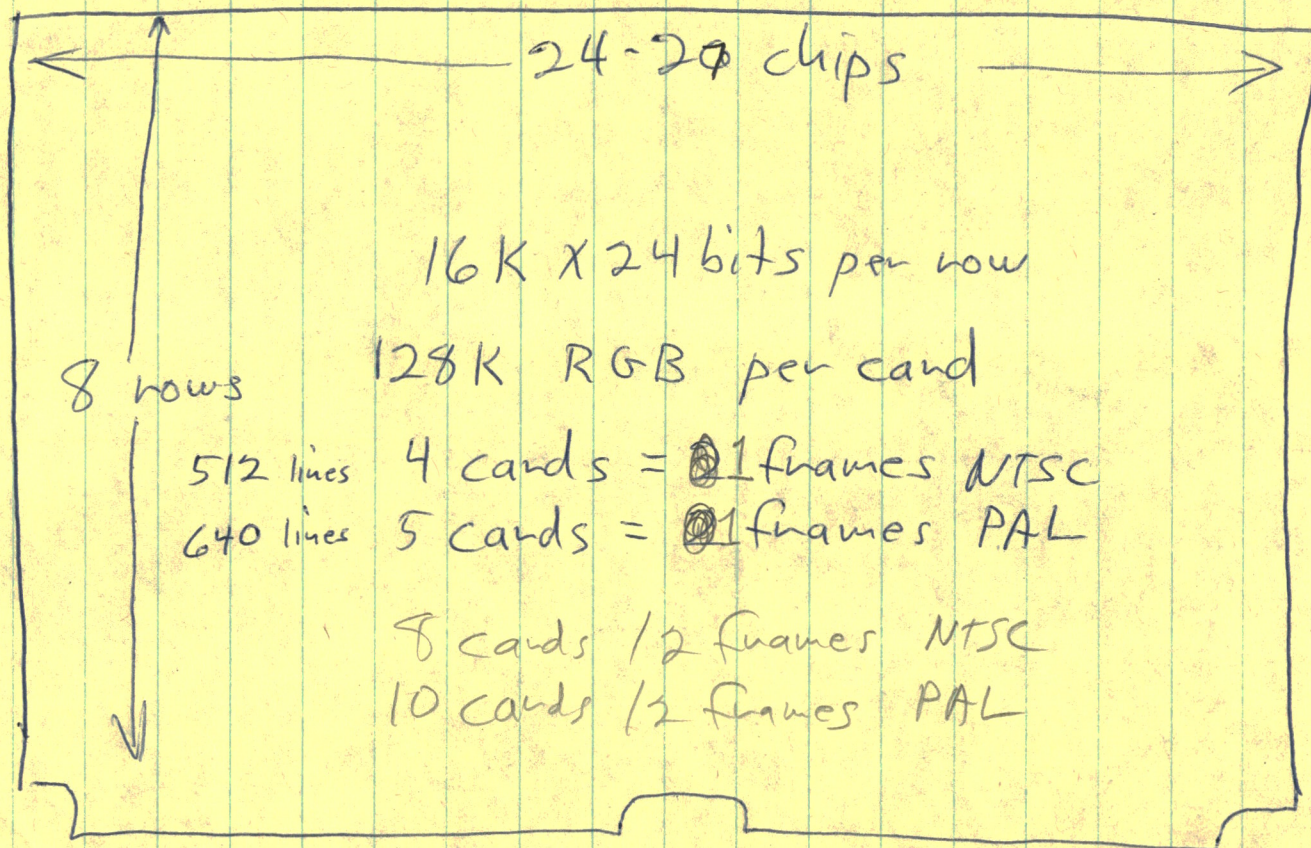
T1- R41C  
 D-1,2 MR250-4  
 R-1 2.5K, 25W  
 Z-1,2 - 1N2846 @ 200V 50W  
 Z3 - 1N2843 @ 150V 50W  
 C1-4 - 50u @ 450V TUA1713



	Freq	period	Active line samples	line period samples	
4 X $F_{sc}$	14.31818 MHz	69.85 ns	752	910	NTSC ↓
SMPTE	14.35 MHz	69.68 ns	754	912	
3 X 256/line	14.62857 MHz	68.36 ns	768	X	
55 ns Max	18.1818 MHz	55.0 ns	954	1155	
1024/line A	19.505 MHz	51.26 ns	1024	X	
1024/line P	16.126 MHz	62.0 ns	847	1024	
682/line A (16K = 24 lines)	13.0 MHz	77 ns	682	X	↓



13 3/4



216 chips/card  
864 chips/frame

1728 N  
2160 P

\$29K N  
\$36,7K P

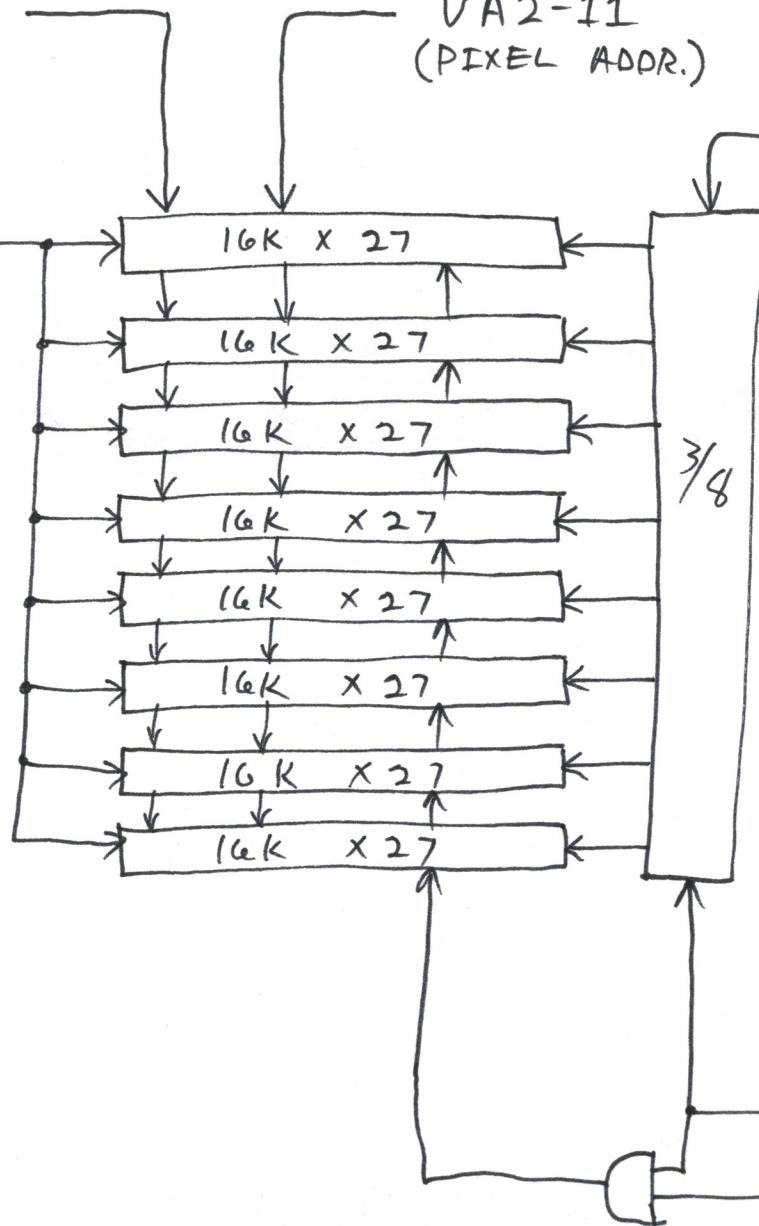


VA0-1  
(BYTE ADDR)

VA2-11  
(PIXEL ADDR.)

VA12-15  
(1 of 16 lines)

VA-16-18  
(1 of 8 rows of 16 lines)

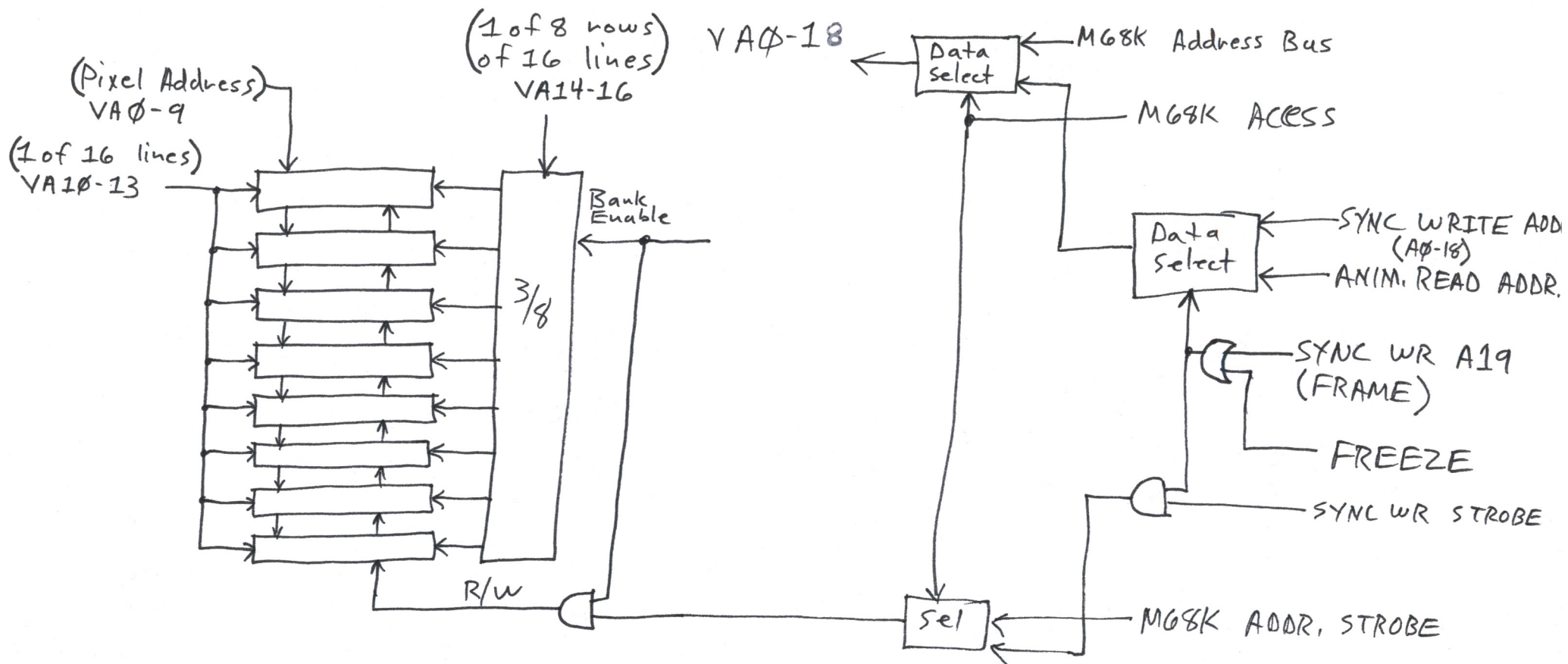


VA19-20  
(1 of 4 128 line)  
Segments

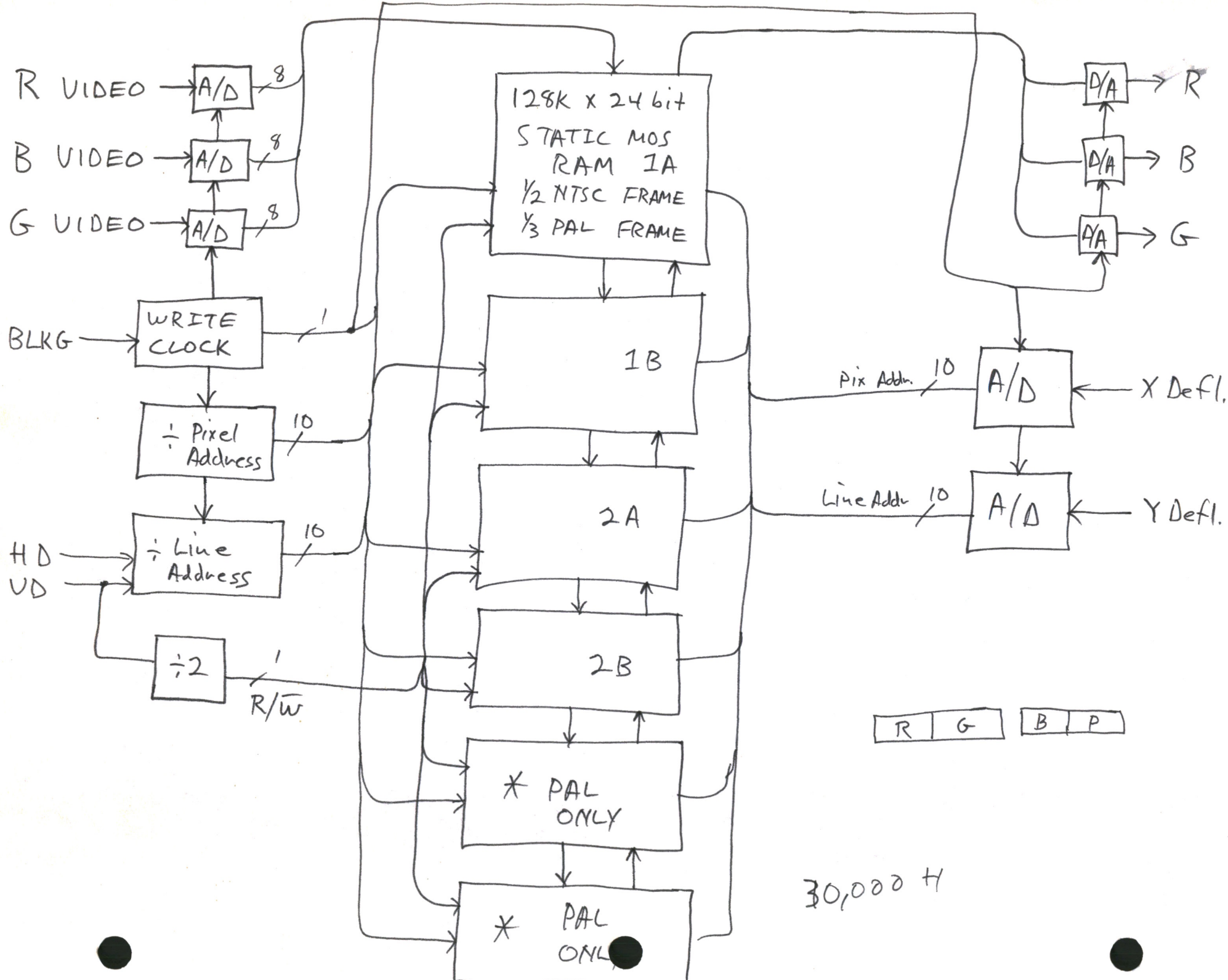
VA-21  
(Field)

VA-22  
(Frame)

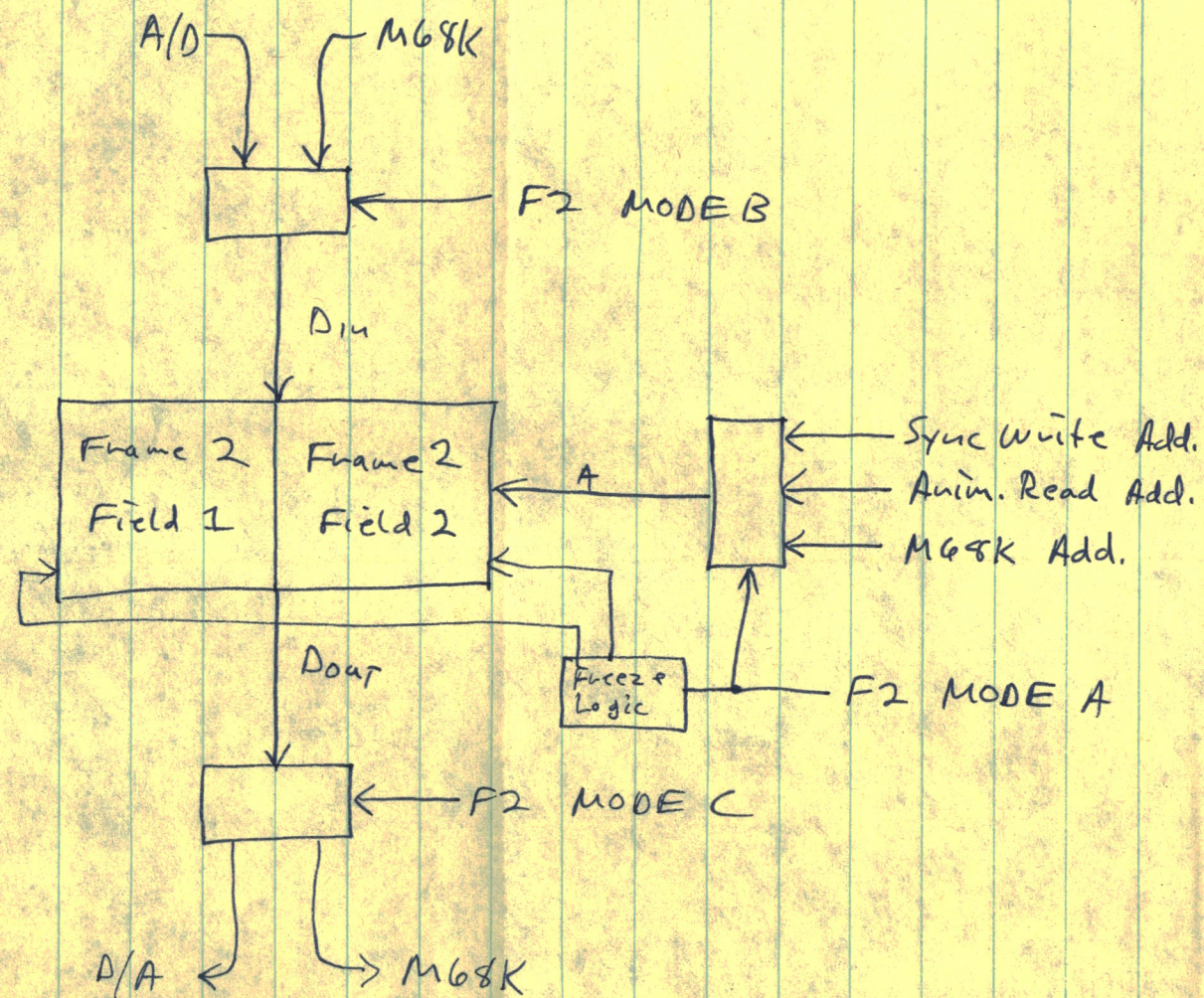
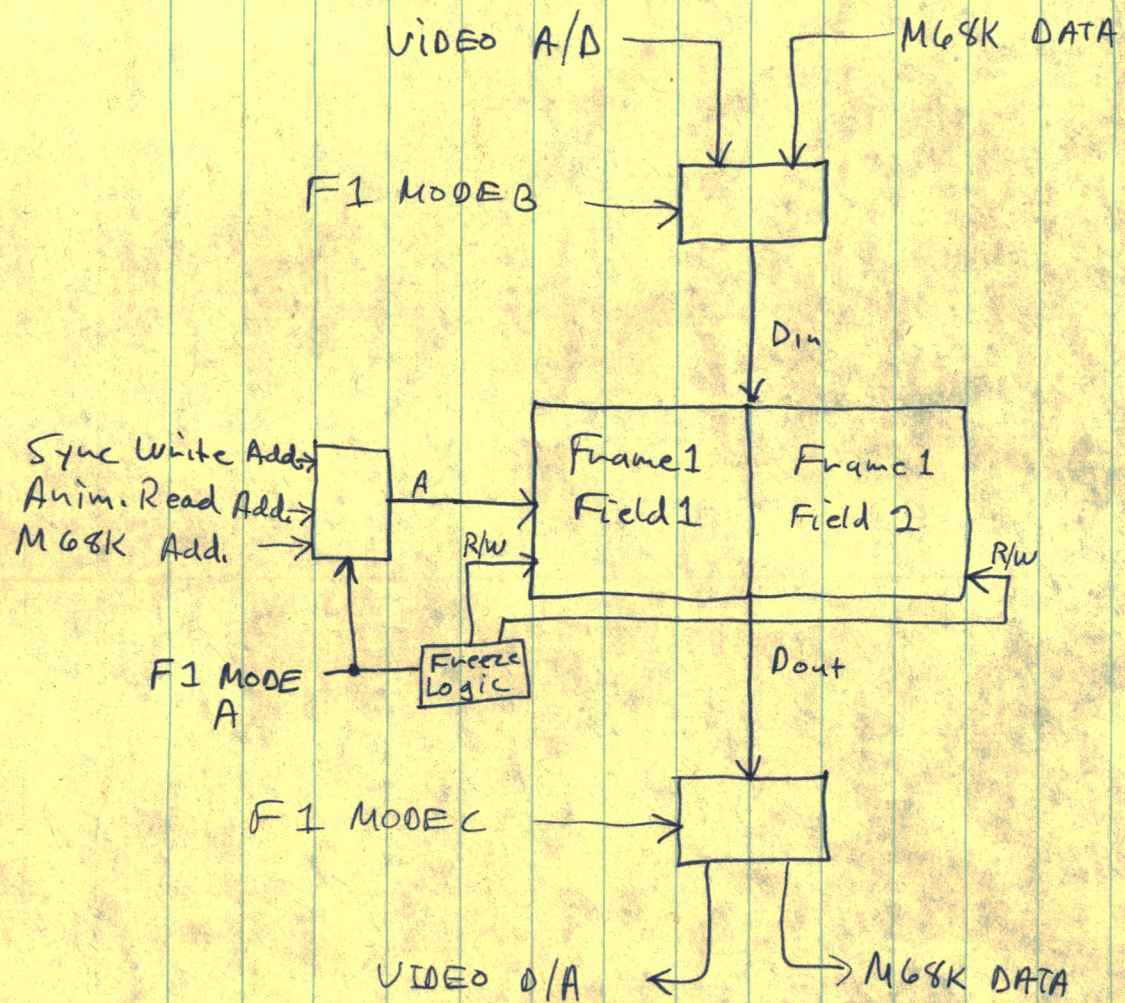




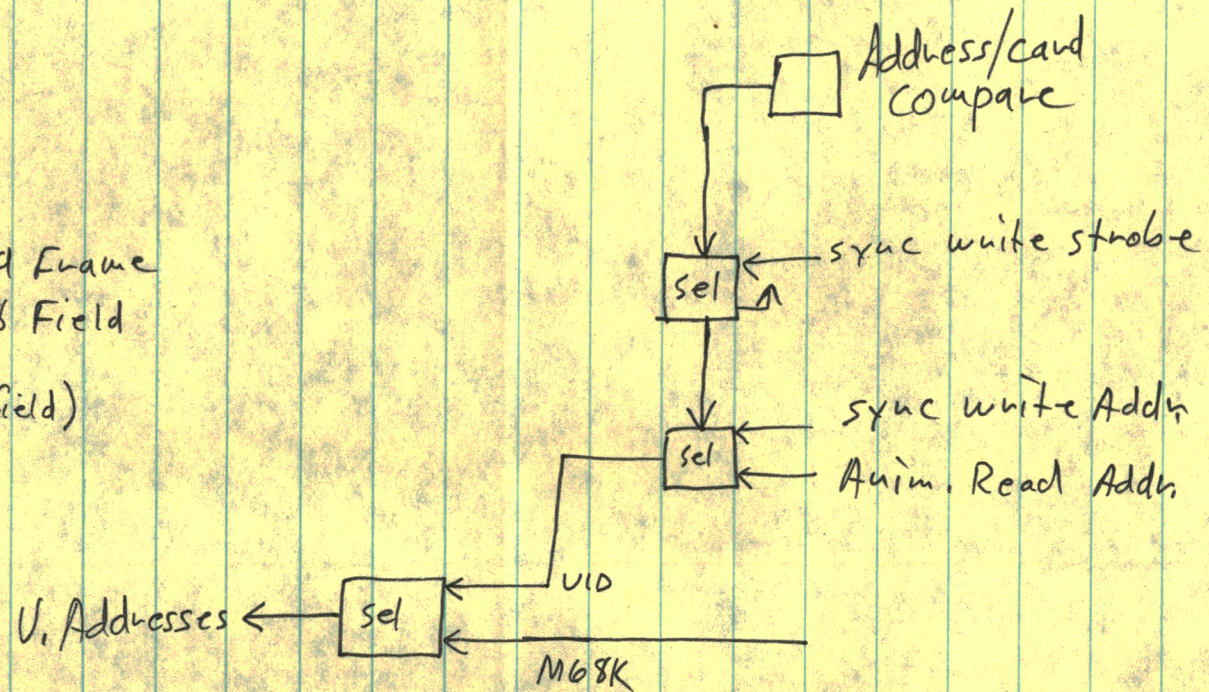
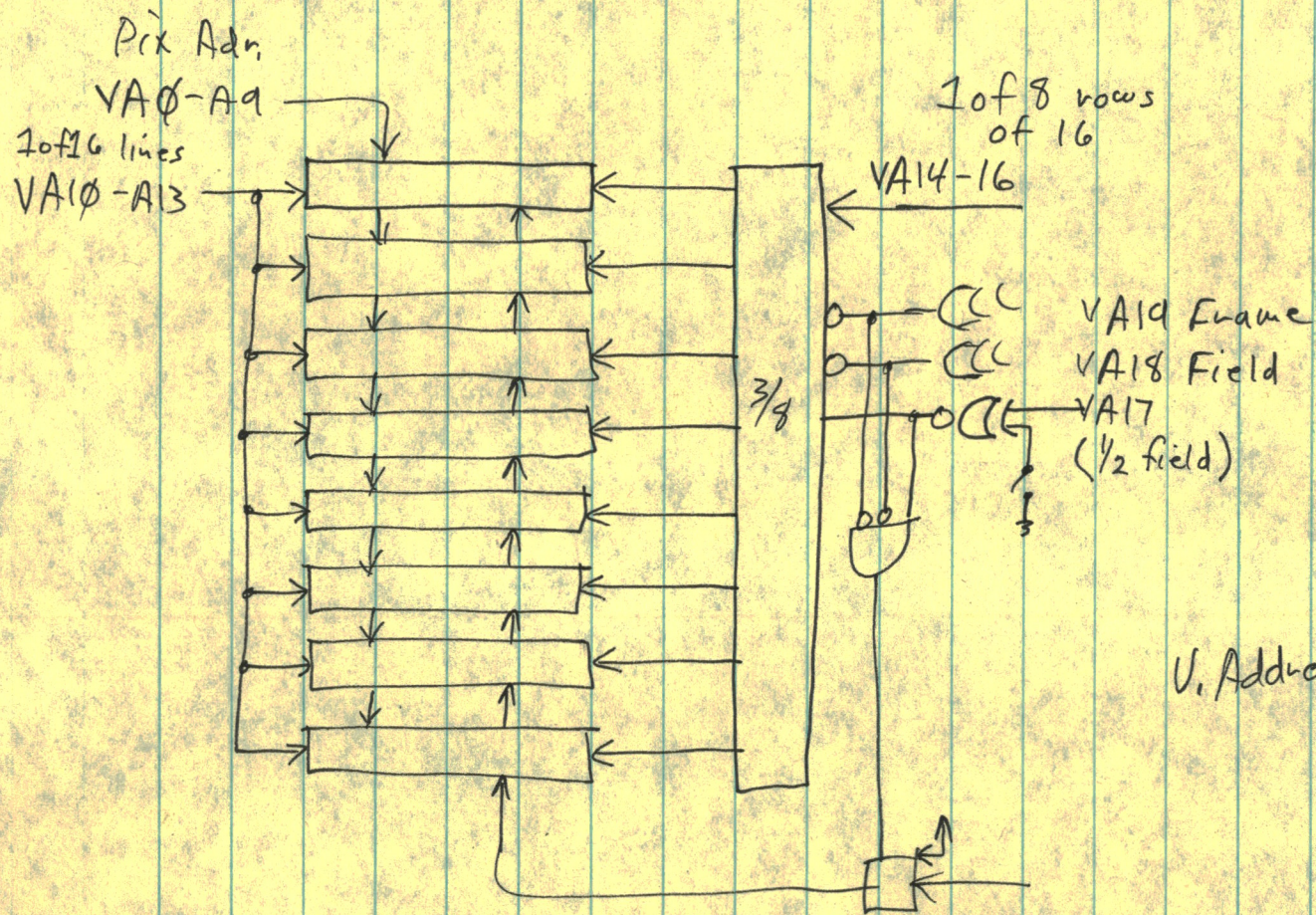




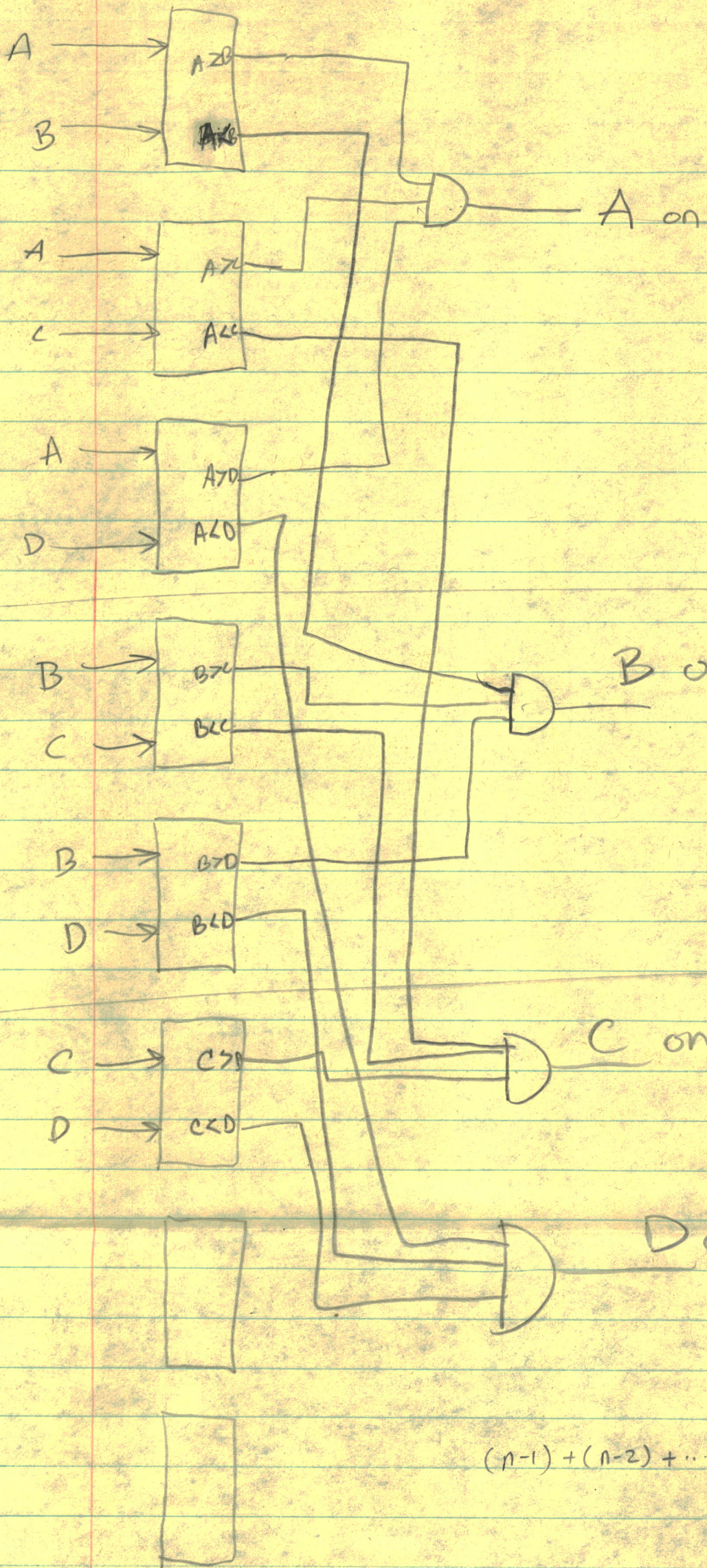












8

36 comp  
8 7 in  
AND:

$$\begin{array}{r} 28 \ 45 \\ 21 \ 36 \\ \hline 55 \ 81 \\ 55 \ 81 \\ \hline 136 \end{array}$$

$$\begin{array}{r} 16 \\ 15 \\ 14 \\ \hline 45 \end{array}$$

$$\begin{array}{r} 13 \\ 12 \\ 11 \\ \hline 36 \end{array}$$

$$\begin{array}{r} 10 \\ 9 \\ 8 \\ \hline 27 \end{array}$$

$$\begin{array}{r} 16 \\ 15 \\ 14 \\ \hline 45 \end{array}$$

$$\begin{array}{r} 16 \\ 15 \\ 14 \\ \hline 45 \end{array}$$

$$\begin{array}{r} 16 \\ 15 \\ 14 \\ \hline 45 \end{array}$$

$$\begin{array}{r} 16 \\ 15 \\ 14 \\ \hline 45 \end{array}$$

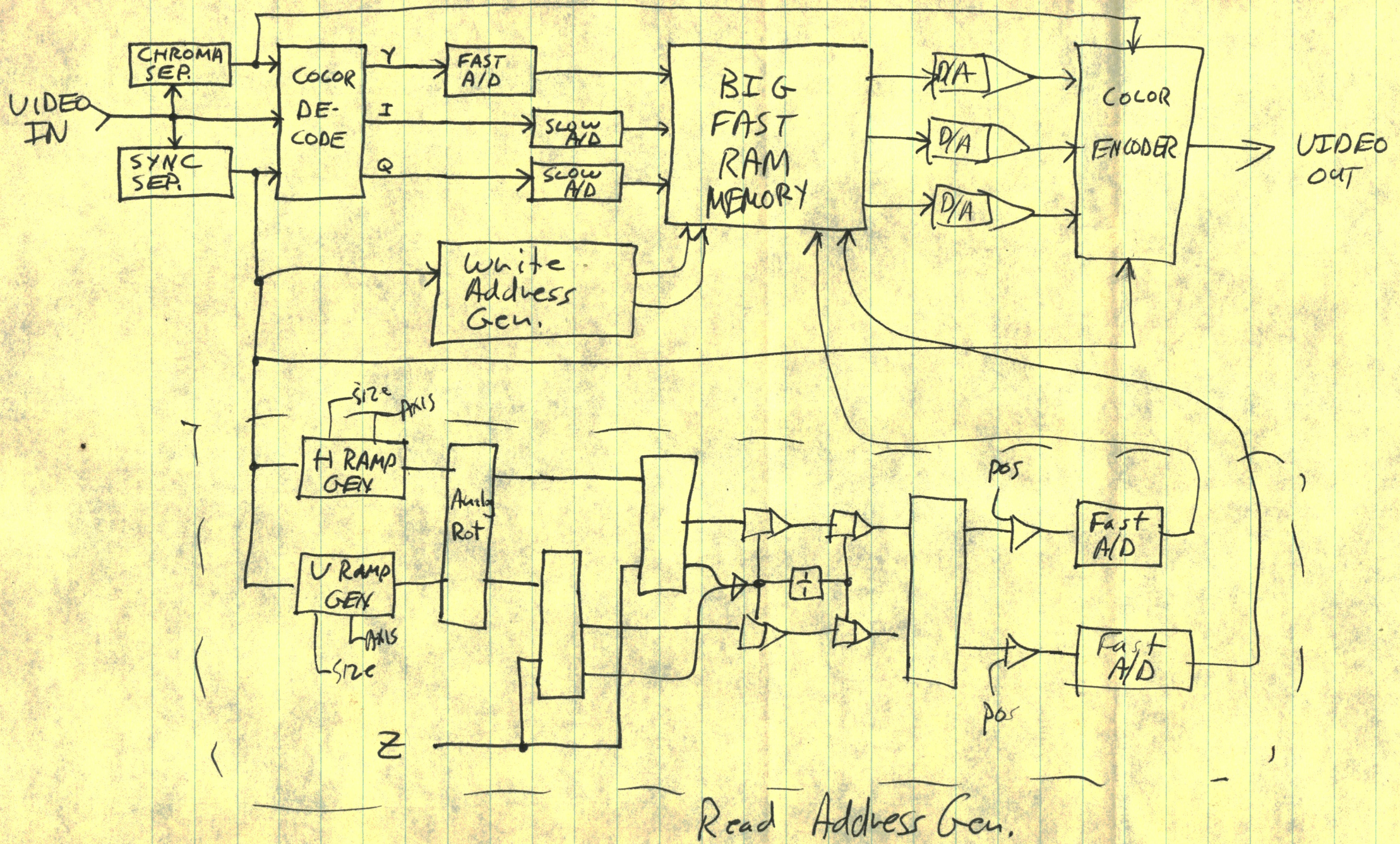
$(n-1) + (n-2) + \dots + (n-n+1)$

$$\sum_{i=1}^{n-1} 1$$

A B C D

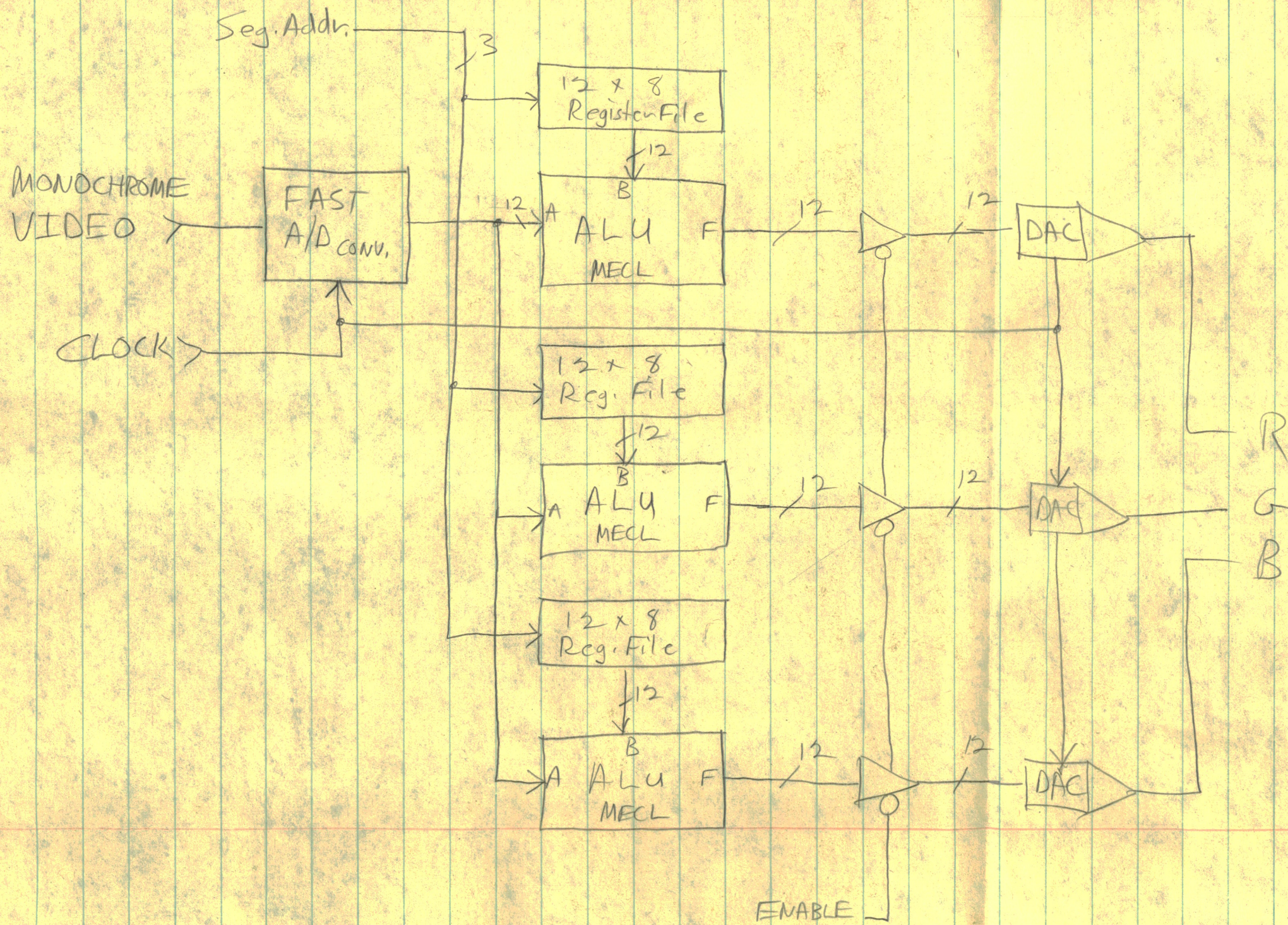
IF  $A > B > C > D$





Digital Framestore Read Address generator - DWS 3.28-81







# Channel Costs

3 Chasses	\$ 9K	27K
1800 Memory chips	\$ 15	30K
50 Multipliers (per seg)	\$ 100	5K / seg
Misc pipe parts		7K / seg

## Boards -

A/D (8 per bdi)		
D/A (8 per bdi)		
Memory (96K/bdi, 4bds/frame, 8bds/chan)		
Translate (2 may be same)	} x 8	76
Rotate (4 different)		6
1/2 Processor (chan) (4 for 8)		96K/bdi
Operator cons (50K)		327K/10K

19.98

5 rows of 27  
4 cards/frame

24  
5  
120



## Setup

VTB-102B (Do mods first)

- No IC's, check for shorts, Gnd to  $\begin{matrix} +5 \\ \pm 15 \\ \pm 12 \end{matrix}$
- Power up board, check supplies.
- Leave on 1 min, make sure no Tantalum caps get hot (they will if in backwards)
- Install Jumpers at J1 + J3, be certain chassis has sync and drives connected and terminated at rear panel, and that they are properly connected to slot 1

Set all  
DIP SW's  
TO "OFF"

Power off - p2 starting at pin 18.

Install U-88, 93, 94, 97, (74LS240) ✓

Install U-92, 95, (74LS244) ✓

Install U-98, 99, (25LS2521) ✓

Install U-81, 82 (74138) ✓

Install U-96 (74260) ✓

Install U-43 (74S38) ✓

Install U-44 (74S74) ✓

Install U-34 (7416) ✓

Install U-66, 68 (74377) ✓

Install U-50, (7428)

- Power on, no chips should get hot
- Through Versabug, enter FFFF data at address FF0000. Both LEDs should light. If not, check for strobe in this order: U99 pin 19, U98 pin 19, U96 pin 6, U43 pin 8, U81 pin 15, U82 pin 15, U50 pin 13



## Setup

where does  
this

Test for UL  
at 47, 65, 68  
(addresses) Square wave

47, 65

②

- off - Install U 48, 67, (74LS377)  
Install U 49 (DAC-80)  
Power up, including  $\pm 15$  supply,  
scope bottom lead of R77.  
Run Ramp program thru Versabug,  
at FF0006. Check for 0 to +5 ramp  
out of DAC.

- off - Install U 62, 63, (25LS157)  
Using short wire wrap jumper, short  
between pins 1 and 12 of U-16's socket.  
Install 8599s or 74189s in:  
U 42, 61, 80, 36, 37, 38, 39, 40, 55, 56, 57  
58, 59, 60, 74, 75, 76, 77, 78, 79.  
Install DAC-80s in U 22, 23, 24, 85, 86, 87.  
Power up, check for hot chips, run  
Ramp program, check for  
ramps at pin 15 of DAC's:
- |      |                  |
|------|------------------|
| U-86 | address = FF0040 |
| U-85 | FF0060           |
| U-22 | FF0080           |
| U-87 | FF00A0           |
| U-23 | FF00C0           |
| U-24 | FF00E0           |



## Setup

3

- Remove jumper from above step.

- check for TTL level sync drives  
at U-88 pins 12, 14, 16.

Power off - Install U 146, 26, (CD4040)

Install U 25, 64 (DM8130)

Install U 51, (CD4046)

Install U 30, 31 (74150)

Install U 71 (74151)

Install U 6, 7, 8, (DM8520)

Install U 45, (7474)

Install U 12, (7433)

Install U 69, (7427)

Install U 70 (74260)

Install U 33 (7400)

Install U 32 (7428)

Install U 4, 5, 13, 14, 15, 16, 17, 18, 19, 20, 52

27, 28, 29 (74123)

Install U 1, 54, 84 (AH0134CN)

Install U-2, 9, 53, 83 (LH0062CD)

Install U-10 (ME34002P)

Install U-3, 11, 21, 35, 72, 73 (NE527)

Install U-89, 91 (74S240)

Install U-90, (74161)



34.7 $\mu$ s

0	0	1
1	1	1
0	1	1
0	0	0

34.5 $\mu$ s

0	1	0
1	0	1
1	0	0
0	1	0

33.8 $\mu$ s

1	0	0
0	0	0
0	1	0
0	1	0

0  
1  
0  
0

0	0	0
1	1	1
0	0	0
0	0	0



# Setup (4)

- up - at FF0000 put data: 00F2  
should get 2 ramp at TP1, Hramp TP3
  - at FF0002 put data: 0000  
should get lower Horiz drive at TP 4 + 5  
(inverted at 5) Set scope to trigger +  
from TP 5 upper trace, display <sup>house</sup> Bars lower.
  - at FF0002 put data: 0001. Adjust  
R30 (LH blanking width) and R31  
(LH blanking start position) see timing chart <sup>#1</sup>
  - at FF0002 put data: 0002. Adjust  
R29 + 28, (see timing chart <sup>#1</sup>)
  - at FF0002 put data: 0003. Adjust  
R26 + 27. (see timing chart <sup>#4</sup>)
  - at FF0000 put data: 00F3.  
at FF0002 put data 0025
- Set Sw 1, 2, 3 as follows:

28.57 KHz = 35 $\mu$ s HH period @ = 945 line NTSC = 1134 line PAL	<div>off</div> <div>on</div> <div>on</div> <div>on</div>	<div>on</div> <div>off <math>\div 10</math></div> <div>off</div> <div>on</div>	<div>off</div> <div>on <math>\div 14</math></div> <div>off</div> <div>off</div>	<div>↑</div> <div>TOP</div> <div>of</div> <div>BOARD</div>
	Sw1	Sw2	Sw3	

Trigger + TP5, scope TP4, set R25 for  
1  $\mu$ s front porch (see timing chart <sup>#2</sup>), set  
R24 for 7  $\mu$ s blanking width (see chart <sup>#2</sup>)  
Set reset, clamp + sample by chart <sup>#2</sup>

29,304 = 34 $\mu$ s Trig beat x10 Adj R11 for stab.	<div>on</div> <div>off</div> <div>on <math>\div 13</math></div> <div>off</div>	<div>off</div> <div>off <math>\div 3</math></div> <div>on <math>\div 3</math></div> <div>on</div>	<div>off</div> <div>on <math>\div 14</math></div> <div>off</div> <div>off</div>
--	--	---	---



# Waveform Setup (5)

- At FF0002 enter data: 00BB  
Trigger - from TP4 <sup>upper trace</sup>, scope TP5 lower trace, set R17 as per timing chart, #3
- At FF0002 enter data: 00BC  
check for waveform per chart, #3
- At FF0002 enter data: 004B.  
trigger - from TP4, scope Bars <sup>upper trace</sup> and TP5, lower trace, adjust R16 to end vertical Blanking just before start of video on bars. (see chart #4)
- At FF0002 enter data: 004C adjust R15 as per chart, #4
- At FF0002 enter data: 004D. -  
adjust R14 as per chart,
- At FF0002 enter data: 0051, verify timing as per chart,
- At FF0000 enter data: 00F3.  
At FF0020 enter data 4B via repeat pgm.  
At FF0004 enter data 00, VR.  
At FF0002 enter data 52. verify <sup>multiple vertical Resets</sup>  
similar to chart, #5 Trigger - on lower trace from TP4, VR. At FF0002 enter data 44, adjust R11 until top trace locks. (x10 mag)  
set R11 in center of lock range.
- At FF0002 enter data 30. Adjust R12 to make trailing edges of both pulses equal.  
~~At FF0000 enter data 30, at FF0002 enter 32.~~  
Adjust R10 to make trailing edges equal.



# Setup

(6)

- At FF0005 enter 0F
- A + FF0000 enter F2
- Adjust R13 as above (falling edge equal)

---

At FF0000 enter F7  
At FF0002 enter 53  
Adjust R8 + R9 as per chart #6

---

At FF0000 enter F7  
At FF0002 enter 34  
Trigger + from TP5, verify 100ns pulse.  
Trigger - from TP4, set scope to display  
1 HH period. verify that TP5 signal remains  
locked. At FF0006 enter 00. verify  
at least 50 (likely 75) pulses per Hires H.  
AT FF0006 enter FFF verify no pulses.  
AT FF0006 enter D00 verify 11 pulses per <sup>on</sup> time of HH  
AT FF0002 enter 34. verify as per  
timing chart 7.

---

Using Repeat program, enter the following  
data at these addresses:

② FF0040	200	② FF0020 000
② FF0060	D00	
② FF0080	200	
② FF00A0	D00	
② FF00C0	200	
② FF00E0	D00	



# Setup

7

Using VERSAbugRO set modes:

- ① FF0000 95
- ② FF0002 56
- ③ FF0004 000
- ④ FF0006 D00

Trigger - from TP4, check TP5 upper trace, TP2 lower. Adjust R86, verify that amplitude of ramp affects timing of UB1 and UB2. See Timing chart #8. Set R86 so Ramp goes 0 to +10 v.

At FF0000 enter 91. Verify that VAL pulse disappears.

At FF0000 enter 9D. Verify that all blanking goes to zero.

At FF0000 enter 95.

At FF0002 enter 36

change scope probe from TP2 to TP3  
change scope rate to 5 $\mu$ s/cm

Adjust R74, verify that amplitude of ramp affects timing of HB1 and HB2  
See timing chart #9. Set R74 so Ramp goes zero to +10 v.

At FF0002 enter 96 Move scope probe to TP1 from TP3. Verify as per timing chart #10.

At FF0000 enter 85. Verify Z Ramp goes to Zero.



# Setup

(8)

- Check for Low-Res Blanking at  
P2-88, Camera Vent. Trigger at  
P2-26, Camera Hor. Trigger at  
P2-28, Camera Blanking at P2-30



V1B 102B TEST AND TRIGGER REGISTER

(2) FF0002 with all Dip Sws off

BYTE FORMAT:

D7 D6 D5 D4 D3 D2 D1 D0

HEX

TP4

TRIG 1 of 8

TEST- 1 of 32

TP5

Low-Res. Horiz Drive	X X X 0 0 0 0 0	00
" " " Blanking	X X X 0 0 0 0 1	01
" " " Reset	X X X 0 0 0 1 0	02
" " " Clamp	X X X 0 0 0 1 1	03
High Res. Horiz Drive	X X X 0 0 1 0 0	04
" " " Blanking	X X X 0 0 1 0 1	05
" " " Reset	X X X 0 0 1 1 0	06
" " " Clamp	X X X 0 0 1 1 1	07
Horizontal Sample pulse	X X X 0 1 0 0 0	08
Low-Res Vertical Drive	X X X 0 1 0 0 1	09
" " Field sample pulse	X X X 0 1 0 1 0	0A
" " Vertical Blanking	X X X 0 1 0 1 1	0B
Camera Vertical Trigger	X X X 0 1 1 0 0	0C
Vertical Interval	X X X 0 1 1 0 1	0D
Multiple Vertical Reset	X X X 0 1 1 1 0	0E
Low-Res Section Reset Blank.	X X X 0 1 1 1 1	0F
High-Res Section Reset Blank.	X X X 1 0 0 0 0	10
Counter Vertical Reset	X X X 1 0 0 0 1	11
Vertical Reset	X X X 1 0 0 1 0	12
Vertical Axis locate	X X X 1 0 0 1 1	13
Z Reset	X X X 1 0 1 0 0	14
Z Blanking	X X X 1 0 1 0 1	15
CRT Blanking	X X X 1 0 1 1 0	16
Section address 1	X X X 1 0 1 1 1	17
Section address 2	X X X 1 1 0 0 0	18
Section address 3	X X X 1 1 0 0 1	19
Section address 4	X X X 1 1 0 1 0	1A
Low-Res. Sync	X X X 1 1 0 1 1	1B
Field Indent	X X X 1 1 1 0 0	1C
Section Vertical Reset	X X X 1 1 1 0 1	1D
VERTICAL AXIS LOCATE ENA	X X X 1 1 1 1 0	1E
Z Reset Enable	X X X 1 1 1 1 1	1F
Low-Res Horizontal Drive	0 0 0 X X X X X	0(1)X
High-Res Horizontal Drive	0 0 1 X X X X X	2(3)X
Low-Res Vertical Drive	0 1 0 X X X X X	4(5)X
Section Reset	0 1 1 X X X X X	6(7)X
Z Reset	1 0 0 X X X X X	8(9)X
Low-Res Field Sample	1 0 1 X X X X X	A(B)X



E3F = .57V	1H
E00 = .65V	2H
DBF = .72V	4H
D7F = .81V	6H
D3F = .88V	9H
D00 = .96V	10H
CBF = 1.04V	12H
C7F = 1.12V	15H
C3F = 1.19V	17H
C00 = 1.27V	19H
BBF = 1.35V	21H
B7F = 1.43V	24H
B3F = 1.51V	26H
B00 = 1.59V	30H
ABF	

UTB 102B  
Z Ramp  
Rates

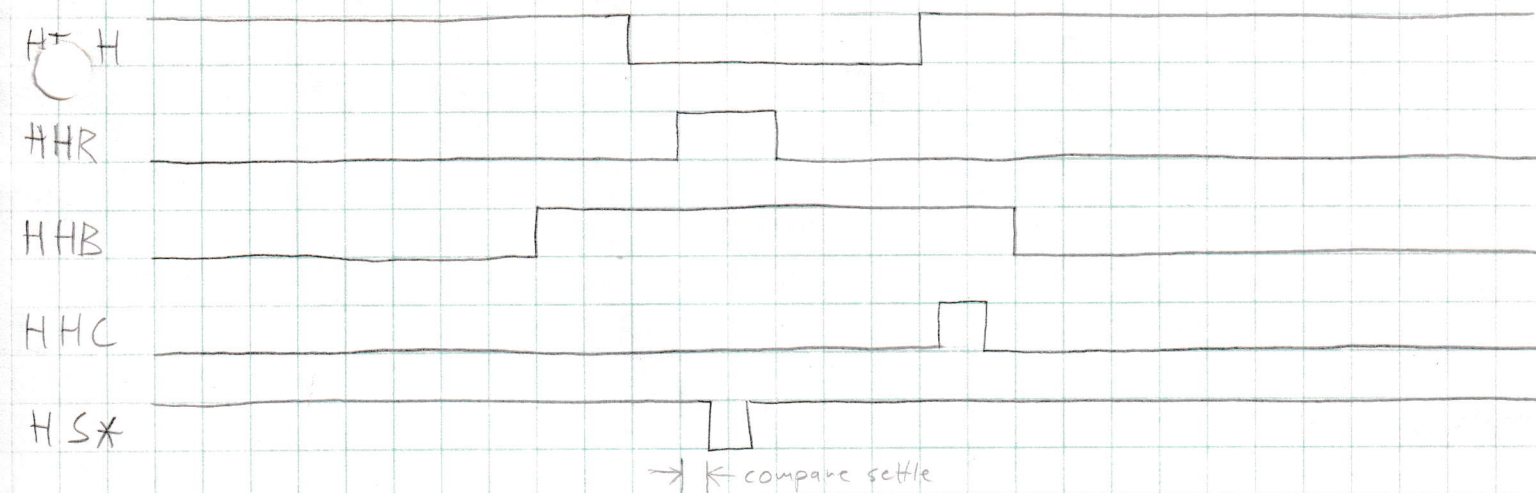
REVISED



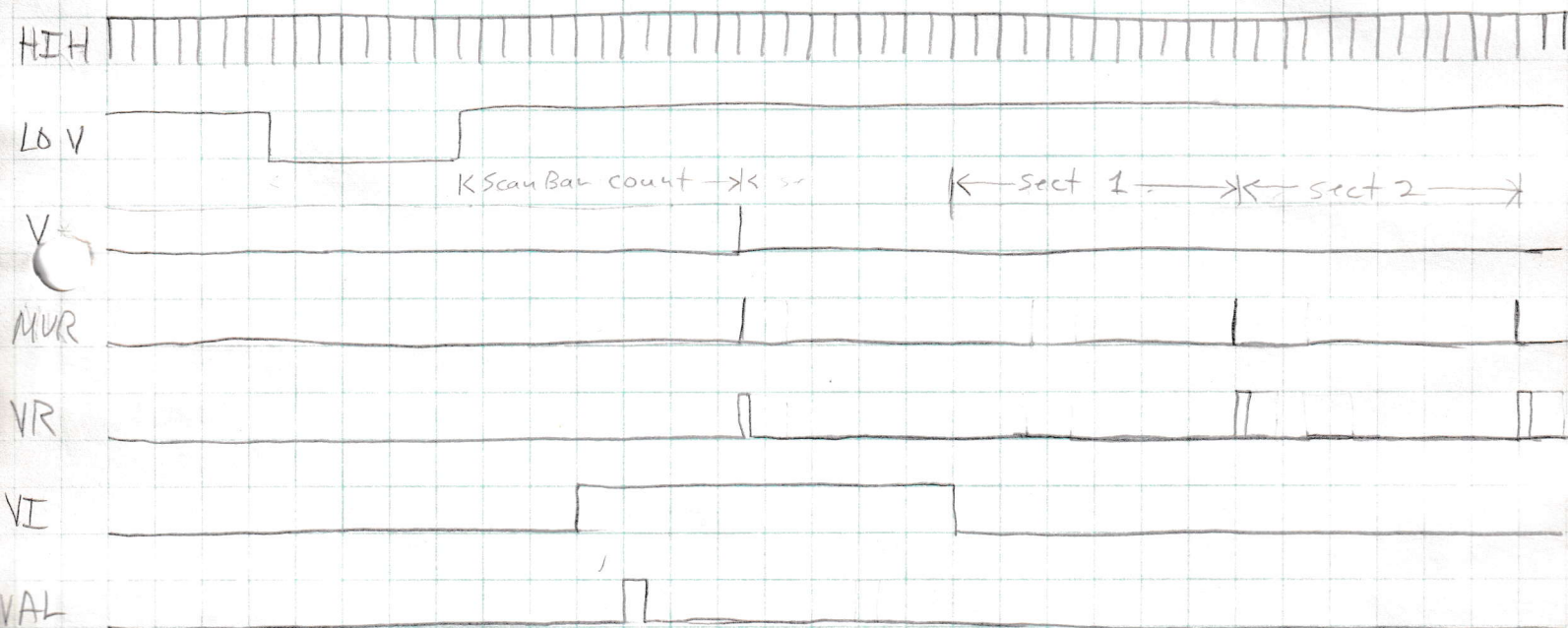




# H. TIMING - HI-RES MODE



# V. TIMING - HI-RES MODE





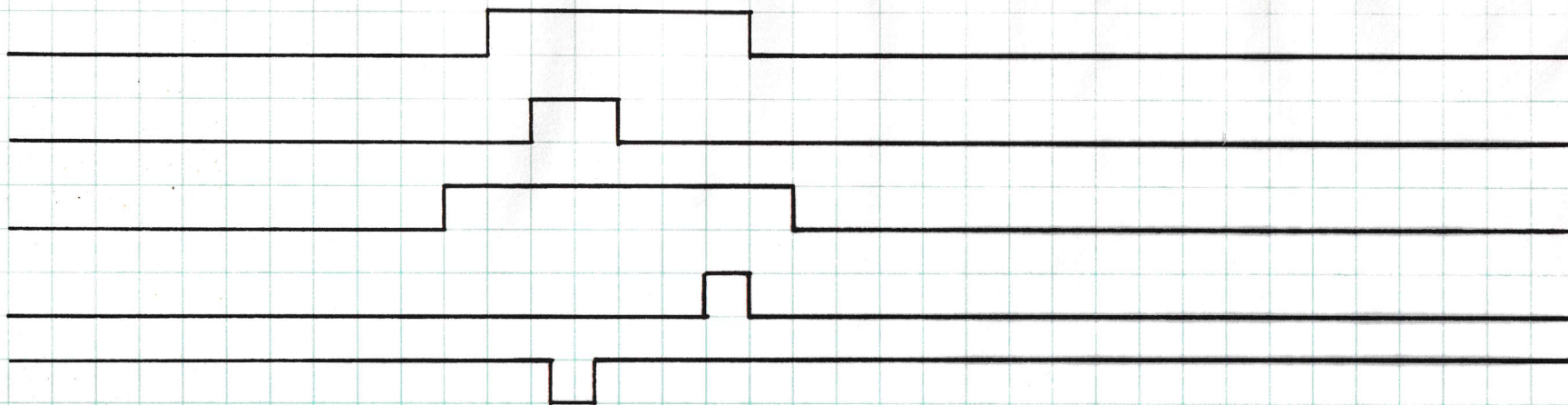
HH

HHR

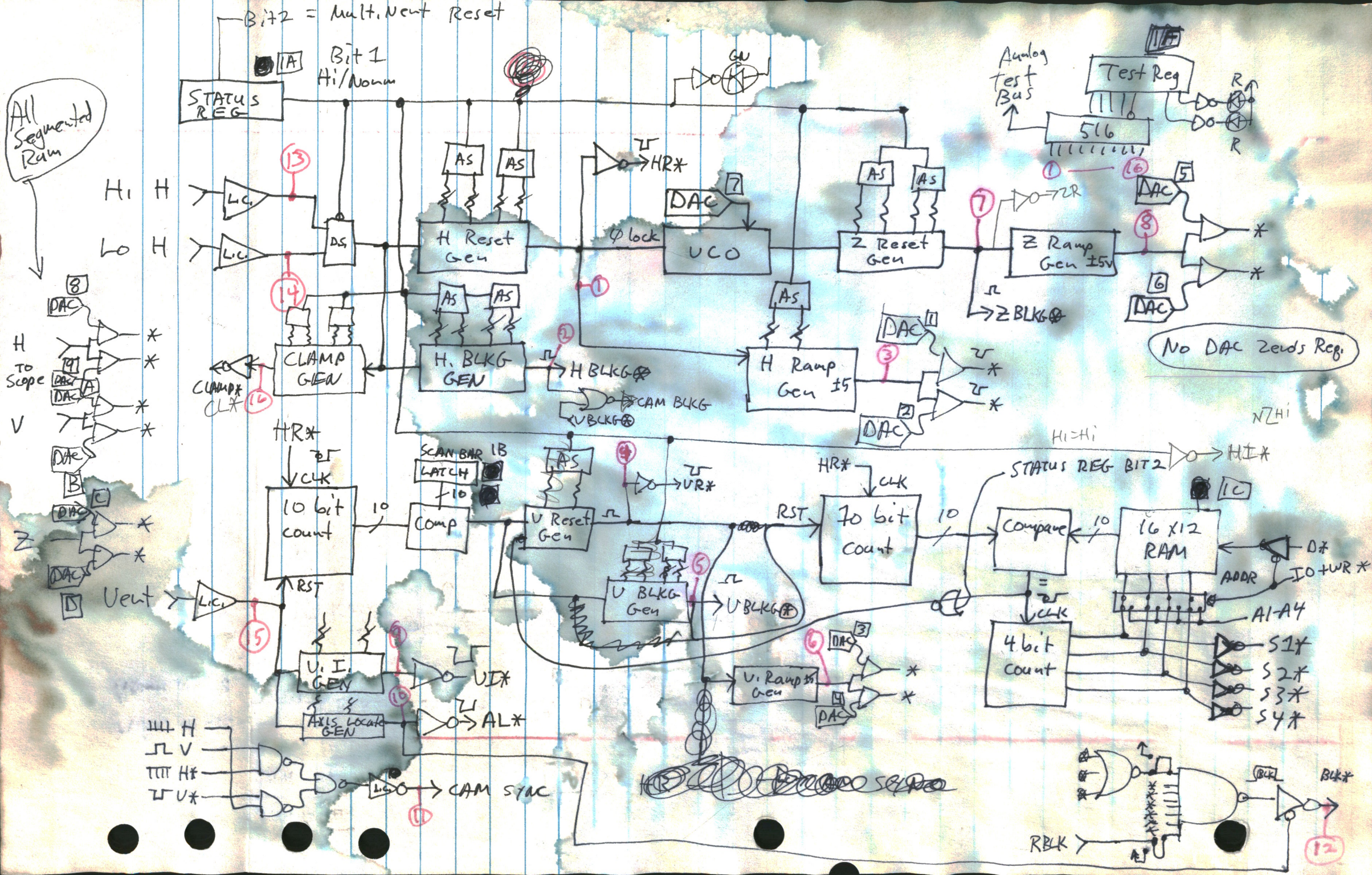
HHB

HHC

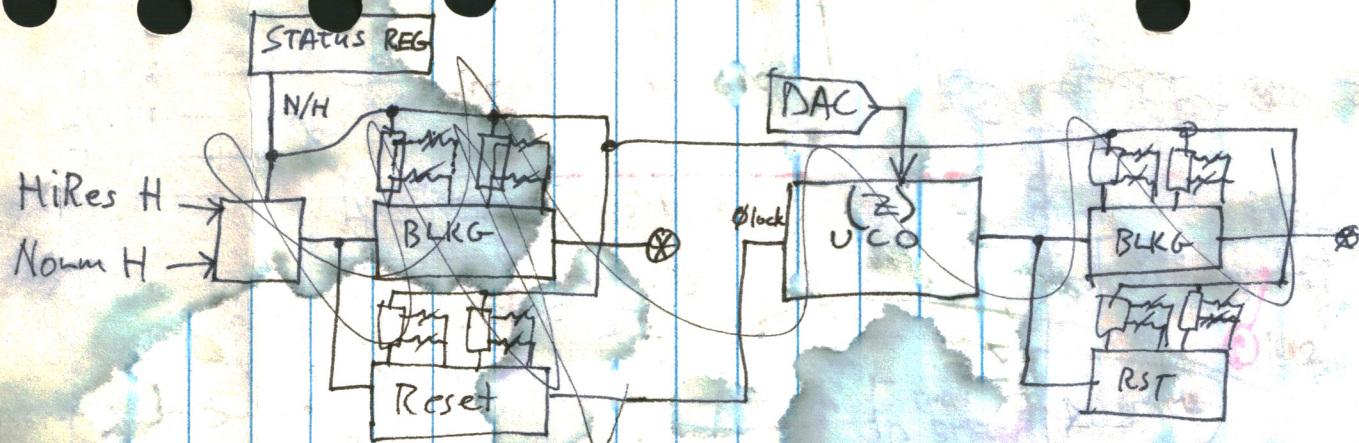
HS\*













1032-7

filename - ~~Board~~ #  
UTB, CL2-10-85  
ordered  
page 1

Refch = 4

PO #1

X5 14  
✓ 70Desc = 74123 Ham28, 29, 19, 5, 18, 20, 14, 13, 14, 4, 27,  
52, 17, 15X5 21  
✓ 105Desc = DM8599 Ham42, 61, 80, 38, 57, 74, 34, 55, 74, 37, 56, 75  
40, 59, 78, 39, 58, 77, 41, 60, 79X5 7  
✓ 35Desc = AD DAC-80 CBIV  
84, 85, 22, 87, 23, 24, 49Analog Dev.  
#2X5 2  
✓ 10Desc = CD 4040 Ham

#1

X5 2  
✓ 10Desc = 25LS157 HamX5 2  
✓ 10Desc = DM8130 HamX5 6  
✓ 30Desc = 74<sup>LS</sup>377 Ham  
65, 47, 66, 68, 67, 48



VJB

Page 2

✓ 4 Desc = 74LS240 Ham  
20 97, ~~88~~, 93, 94

#1

✓ 2 Desc = 745240 Ham  
10 89, 91

✓ 1 Desc = 7416 Ham  
5 34

✓ 2 Desc = 7428 Ham  
10 50, 32

✓ 1 Desc = 7400 Ham  
5 33

✓ 1 Desc = 7427 Ham  
5 69

✓ 2 Desc = <sup>LS</sup>74260 Ham  
10 70, 96

✓ 1 Desc = 74161 Ham  
5 90



VTB

P3

11 Desc = CD4046 Ham  
5 51

#1

16 Desc = NE527 Ham  
30 72, 73, 21, 35, 11, 3

4 Desc = LH0062 CD Ham  
20 83, 53, 2, 9

3 Desc = AH0134 Ham  
15 84, 54, 1

1 Desc = MC34002P Ham  
5 10

1 Desc = 7433 Ham  
5 12

2 Desc = 74574 Ham  
10 44, 45

1 Desc = 74538 Ham  
5 43



VTB

P4

↓ 3 Desc = DM8520 Ham  
15 6, 7, 8

#1

↓ 1 Desc = 74151 Ham  
5 71

↓ 2 Desc = 74150 Ham  
10 30, 31

↓ 2 Desc = 25LS2521 Ham  
10 99, 98

↓ 2 Desc = 74<sup>LS</sup>138 Ham  
10 81, 82

Refchar = RP

#3

↓ 3 Desc = SIP, 2K x 8  
15 ~~MAN = MEPCO~~

MAN = MEPCO

Ham

↓ 3 Part # = 9510E13A 2201GL002  
7, 2, 3



UTB

p5-

Refch = SW

Desc = 4 position ✓ DIP sw.  
1, 2, 3

Roy-Yale on  
pacific

Desc = 8 position ✓ DIP sw  
4

Refch = R

Ham

MEPCO

Desc = 330  $\Omega$  1/4w 590  
88, 90, 92, 94, 69, 68

CR5000 series

#3

Desc = 1K $\Omega$  1/4w 590

89, 91, 93, 95, 81, 83, 84, 82, 59, 71, 73, 70,  
41, 42, 4, 5, 63, 65, 47, 60, 61

Desc = 2.2K $\Omega$  1/4w 590

43, 66, 67, 79, 45, 50,

Desc = 4.7K $\Omega$  1/4w 590

56, 32, 76, 49, 54, 55, 58, 51, 46, 34, 35

96



VTB

VTB

TRIMPOTS

R8-31

VALUE

R 8 10 K

9 10 K

10 10 K

11 50 K

12 5 K

13 5 K

14 5 K

15 10 K

16 10 K

17 5 K

18 10 K

19 50 K

20 10 K

21 10 K

22 10 K

23 50 K

24 10 K

25 10 K

26 10 K

27 10 K

28 10 K

29 50 K

30 10 K

31 10 K



VTB

P7

2 Desc = 1.5K 1/4w 590  
46, 44

#3

51 Desc = 8.2K 1/4w 590  
53

#4

8-31

~~scribble~~

MAN = BOURNS  
PART# = Type 3006

4 Desc = 5K ohm pot  
12, 13, 15, 14, 17

Desc = 10K ohm pot

17 16, 22, 28, 24, 25, 30, 31, 21, 20, 26, 27,  
85 14, 15, 8, 9, 10, 18

4 Desc = 50K ohm pot  
19, 23, 29, 11

2 Desc = 10K ohm trimmer  
10 Part # = Bourns Type 3329  
86, 74



VTB

Kemet p8

#5

Refchr = C

✓ 23 Descr = 1uf 25V

115 Man = Kemet

Part# = T392A105K025AS

79, 77, 80, 121, 122, 123, 118, 119, 120, 38, 39, 40  
124, 125, 126, 41, 42, 43, 44, 45, 46, 1, 23

1 Descr = 10uf 25V

✓ 5 Man = Kemet

Part# = T392C106K025AS

11

✓ 84 Descr = .1uf 50V

420 Man = Kemet

Part# = C323C104M5R5CA

25, 16, 14, 17, 83, 24, 117, 64-69, 89-94  
110-115, 15, 18, 21, 24, 27, 30, 33, 36, 8-10  
47, 48, 50, 53, 57, 59, 60, 61, 62, 63, 70-76  
78, 81, 82, 85, 95-108, 127-138



VTB

P1

Kemet (5)

✓ 4 Descr = .01  $\mu$ f 50V  
20 Part# = ~~C323C103M2G5CA~~ C323C103M2G5CA  
7, 34, 20, 22

✓ 8 Descr = 1000 pf 200V  
80 Part# = C323C102M2<sup>G</sup>5CA  
52, 56, 32, 6, 31, 139, 49, 28,

✓ 2 Descr = ~~560~~ 560 pf 200V  
10 Part# = C323C561M2<sup>G</sup>5CA  
87, 88

✓ 6 Descr = 100 pf ~~200~~ 200V  
30 Part# = C323C101K2G5CA  
55, 58, 29, 35, 19, 51

✓ 4 Descr = 39 pf 200V  
20 Part# = C323C390K2G5CA  
4, 5, 84, 86, 2

✓ 1 Descr = 18 ~~30~~ pf 200V  
5 Part# = C323C180K2G5CA  
81



WTB

~~RODA~~

P10

#1

order with  
I'C's

Refch = CR

↓ 9 Desc = 1N914 Diode  
45 1-9

Refch = LED

↓ 1 Desc = Red 90° LED  
1

↓ 1 Desc = Green 90° LED  
2

Roy  
Xaleon  
Pacific

? Refch = TP

Desc = Test point

DAVE



UTB

p6

#3

✓  
5 Desc = 470  $\Omega$   $\frac{1}{4}w$  5%  
25 77, 57, 33, 7, 1,

✓  
2 Desc = 47K  $\frac{1}{4}w$  (1%) SPR-5000 series  
10 34, 39,

✓  
3 Desc = 75K  $\frac{1}{4}w$  (1%) SPR-5000 series  
15 37, 38, 40

✓  
3 Desc = 10  $\Omega$   $\frac{1}{4}w$  5%  
15 87, 80, 3

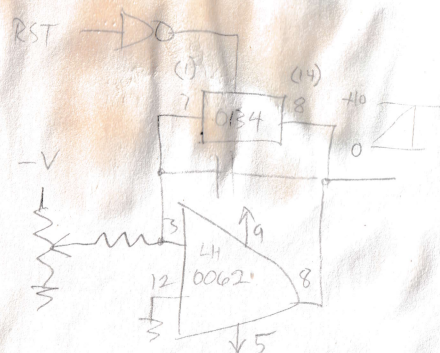
✓  
3 Desc = 15K  $\frac{1}{4}w$  5%  
15 73, 2, 52

✓  
1 Desc = 150K  $\frac{1}{4}w$  5%  
5 85

✓  
2 Desc = 20K  $\frac{1}{4}w$  5%  
10 78, 6

✓  
2 Desc = 3.3K  $\frac{1}{4}w$  5%  
10 62, 64,







VTB

MISSING PARTS

~~R14~~ ~~5K~~ ~~TRIM POTS~~

~~R17~~ ~~"~~

~~R23~~ ~~50K~~ ~~TRIM "~~

~~R29~~ ~~50K~~ ~~TRIM "~~

~~C4-5~~ ~~39pF~~ ~~NEED 3~~

~~C11~~ ~~10uF~~ ~~" 1~~

~~C26~~ ~~.22uF~~ ~~" 2~~

~~C84~~ ~~39pF~~ ~~2~~

~~C86~~ ~~39pF~~ ~~2~~



# Documentation Files

User 2000

BOARDS.DC

User #	Board #	Description
1000	UCI 100A,FX	Communications Board, Fixes
"	" .MW	" " Multiwire
"	" .DC	" " Documentation
1001	VDG 100A,FX	Display Generator Fixes
"	" .MW	" " Multiwire
"	" .DC	" " Documentation
1002	VUG 100A,FX	Vector " Fixes
"	" .MW	" " Multiwire
"	" .DC	" " Documentation
1003	UCC 100A,FX	Console Connector Fixes
"	" .DC	" " Doc —
1004	VAO 100A,FX	Animation Oscillator Fixes
"	" .DC	" " Doc —
1100	VTB 102,FX	Timing + Blanking Fixes
"	" .DC	" " Doc —
1101	UCB 101A,FX	Colorizer Fixes
"	" .DC	" " Doc —
1102	URG 100A,FX	Raster Generator Fixes
"	" .DC	" " Doc —
1103	VRM 101A,FX	Rotation Matrix Fixes
"	" .DC	" " Doc —
1104	UCR 101A,FX	CRT Driven Fixes
"	" .DC	" " Doc —
1105	VID 101A,FX	Video Board Fixes
"	" .DC	" " Doc —
1106	COHU,FX	COHU MOD5



Board	Space	Base Addr.
Floppy Controller	512 bytes	FF0000
Floppy Expansion	3.5K	
Timing + Blanking	512 bytes	FF1000
Raster Gen	1K	FF1400
Rotation Matrix	1K	FF1800
CRT Driver	1K	FF1C00
Video Board	1K	FF2000
OSC 1	1K	FF2400
" 2	1K	FF2800
" 3	1K	FF2C00
Colorizer 1	1K	FF3000
" 2	1K	FF3400
" 3	1K	FF3800
" 4	1K	FF3C00
" 5	1K	FF4000
" 6	1K	FF4400
" 7	1K	FF4800
" 8	1K	FF4C00

Comm I/O	64 bytes	FFC000
Console	64 bytes	FFC100



Board	Space	Base
Graphics 1	2K	E00000
Graphics 2	2K	E01000
Graphics 3	2K	E02000
Graphics 4	2K	E03000
Vector Gen.	2K	E08000
Communications	16K	E10000



## Setup, URG

Load 7FF (2047) @ FF1400 - FF15BE

Load 0 @ FF1580 - FF15BE

Be sure BFF @ FF1020 (single section)

Table 1 → Zero all dac's as per table 1,  
Scope TP-15, trim R56 for Zero Ramp.

Trim R59<sup>(1)</sup> for Zero offset.

Scope TP-14, Trim R55 for Zero Ramp,

Trim R63<sup>(2)</sup> for zero offset

Scope TP-13, put 10 (17) at FF1000

put ~~000~~ ~~FFF~~ @ FF1000, adj R57<sup>(4)</sup> for  
Zero ramp, adj R67<sup>(3)</sup> for offset

Load 000 @ FF1400, scope TP 15

Load 0 @ FF1000, 2nd trace to Top  
of J-4, Jumper removed,Load 0 ~~FFF~~ @ FF14E0, Adj R79 for  
hi-low transition just below Rail, (fig 1a)Load ~~FFF~~ @ FF14E0, Adj R78 for  
hi-low trans just above rail (fig 1b)

Reload 7FF @ FF14E0 + FF14C0

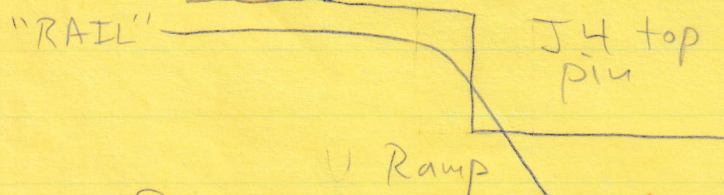


fig 1a



fig 1b

Same for H ramp. <sup>set 0</sup> @ FF1500 + FF1520, scope TP14,

Adjust R80. set FF1520 to FFF, adjust R81.

(Reload 7FF at FF1500 and FF1520) → Same for Z ramp, set 0 @ FF1540 + FF1560, 10 at FF1000

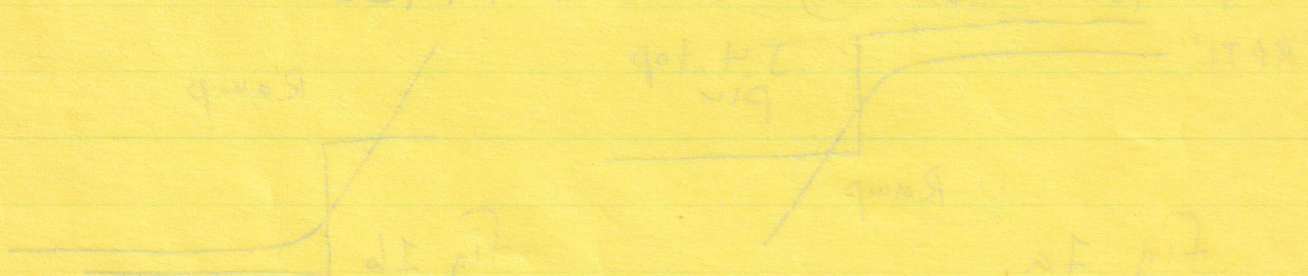
Adjust R84, load FFF @ FF1560, Adjust R83.



- Vertical Axis Locate:  
trigger scope on vertical set 4 at  
FF1000, adjust R16 for 0 to +5  
ramp during vertical Interval at  
TP 13, 14, 15.

End.

- External Amplitude Multiplier balance -





# VRG

## Table 1

Address	IC	Scope	Adjust	Function
FF1400	U30	TP7	R60	V Size Ampl.
FF1420	U31	TP8	R64	H Size Ampl.
FF1440	U32	TP9	R68	Z Size Ampl.
FF1460	U33	TP10	R71	V Axis Ampl.
FF1480	U34	TP11	R72	H Axis Ampl.
FF14A0	U35	TP12	R73	Z Axis Ampl.
FF14C0	U13	TP6	R56	V Size
FF14E0	U18	TP1	R59	V Axis
FF1500	U12	TP5	R55	H Size
FF1520	U9	TP2	R63	H Axis
FF1540	U11	TP4	R57	Z Size
FF1560	U10	TP3	R67	Z Axis
FF1580	D0-4	U76+94		V Size Ext
	D5-9	U78+96		H Size Ext
	D10-D13	U80+98		Z Size Ext
FF15A0	D0-4	U72+95		V Axis Ext
	D5-9	U79+97		H Axis Ext
	D10-D13	U81+99		Z Axis ext

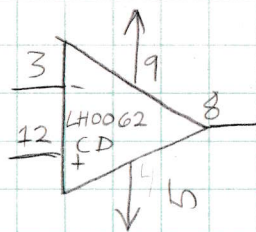


VRG-101A

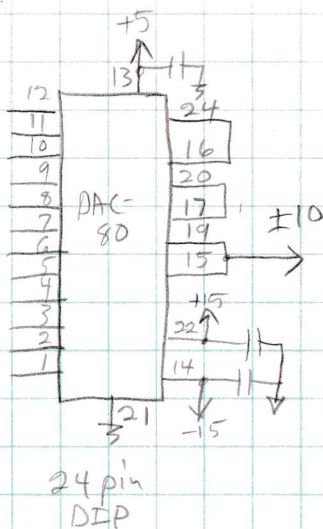
Problem: Pin 4 connected to -15

Solution: change -15 to pin 5

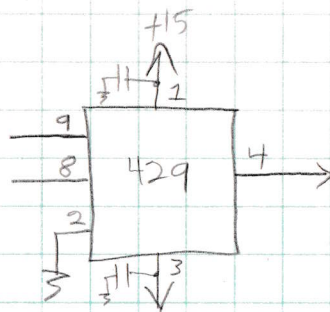




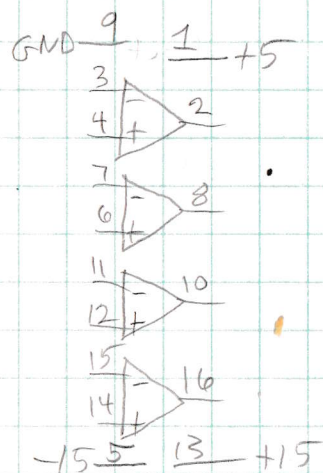
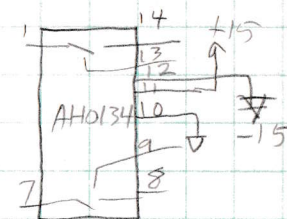
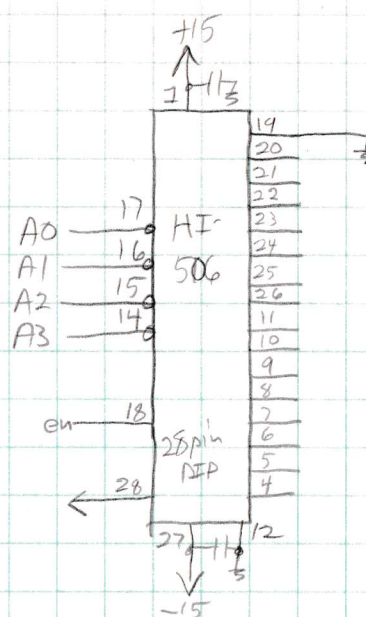
14 pin  
DIP



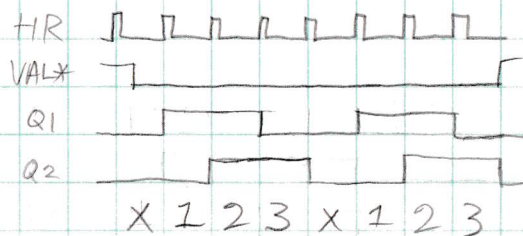
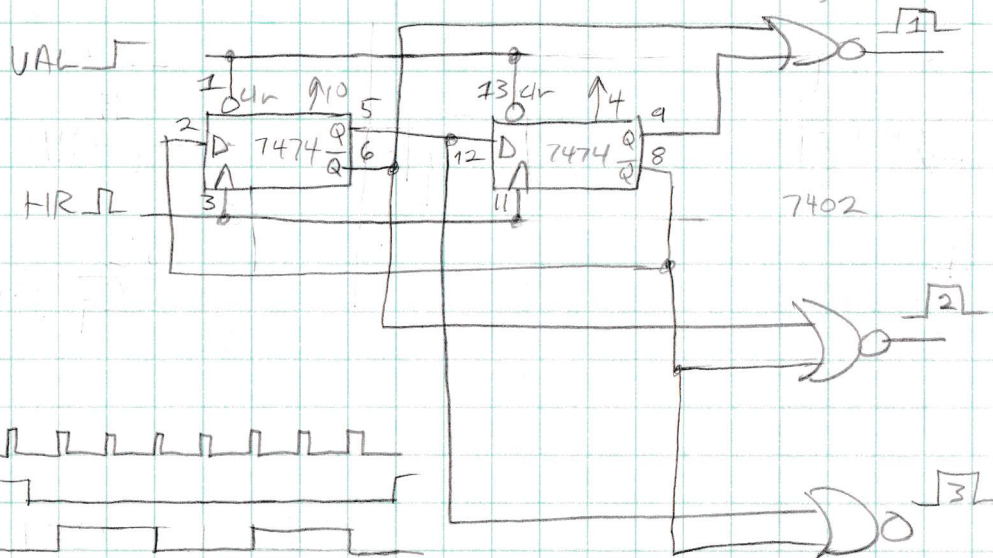
24 pin  
DIP



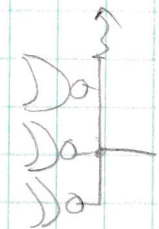
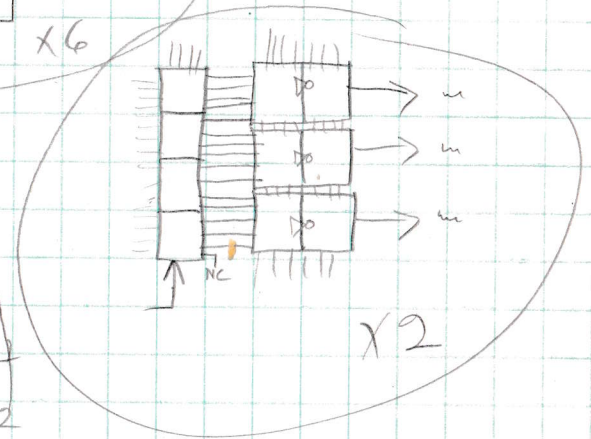
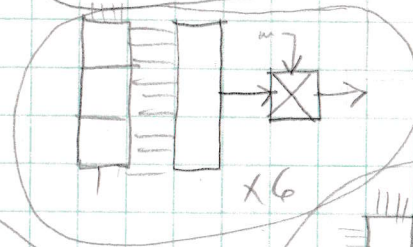
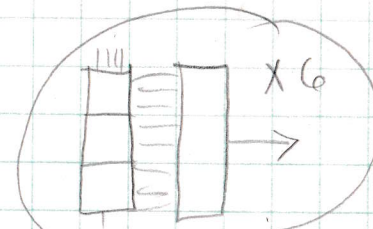
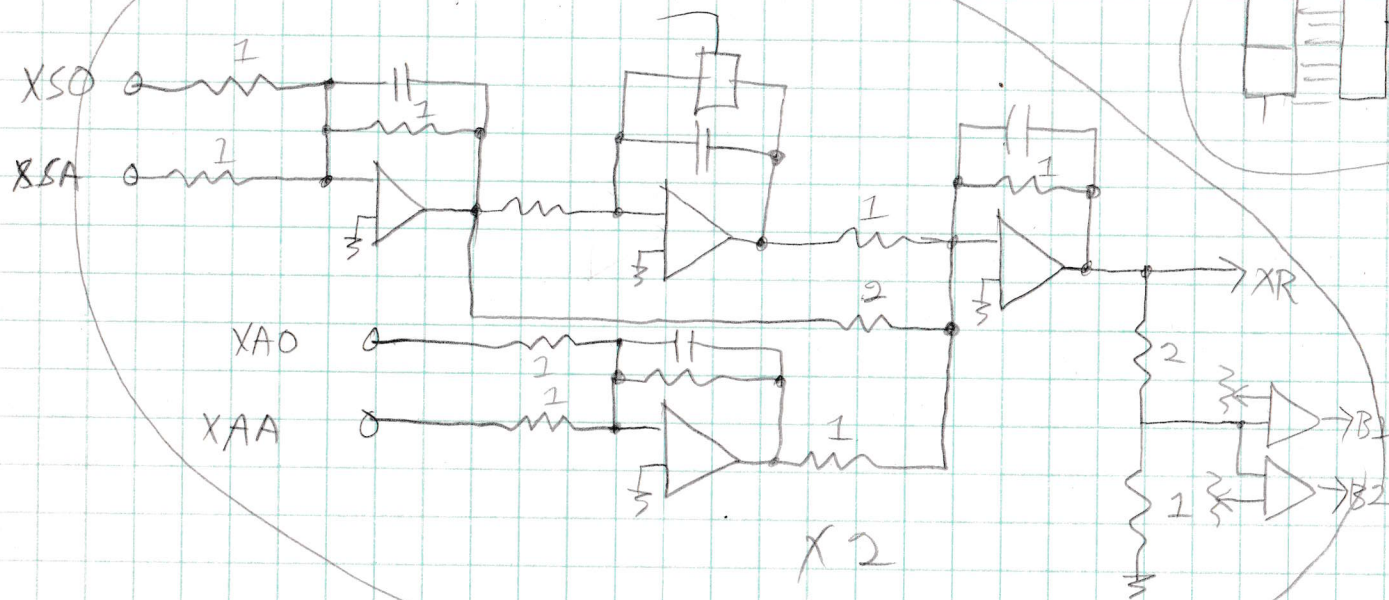
1.51"x1.51"  
oddball package



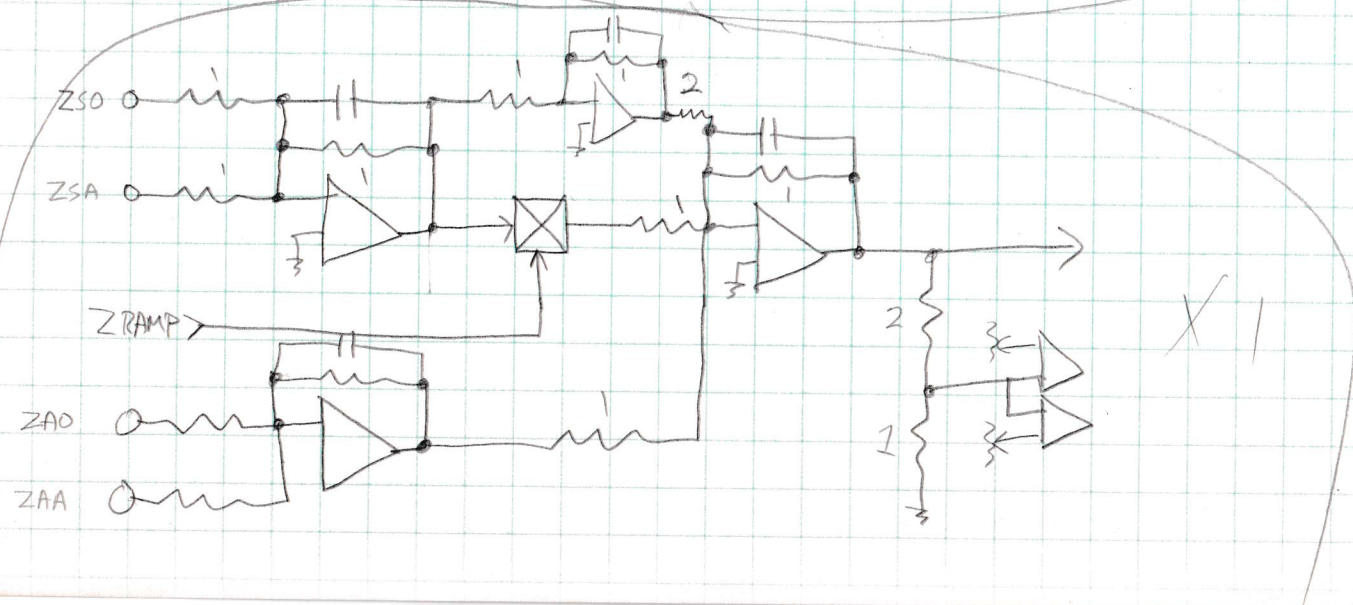
4925







Raster Gen.

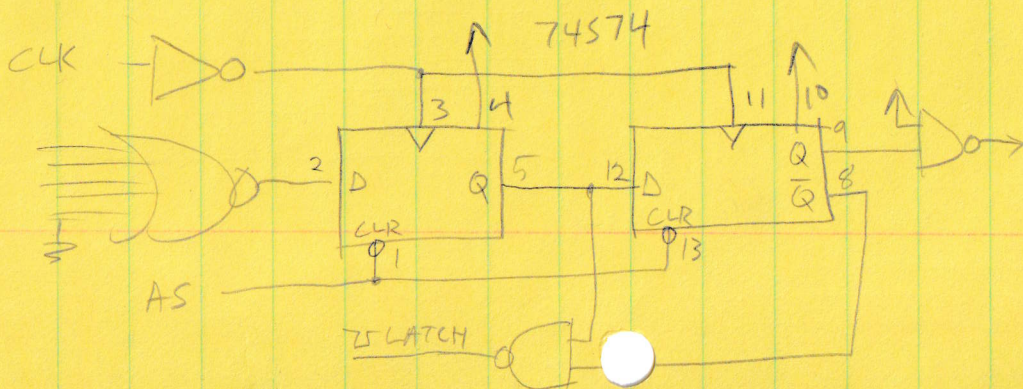
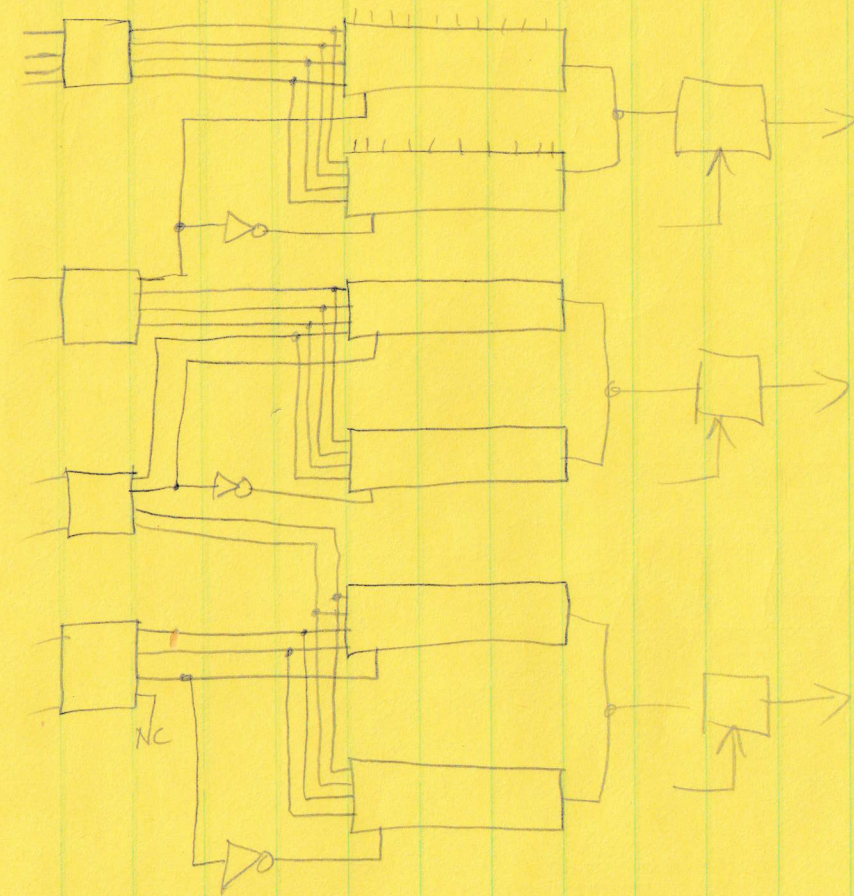




Not X

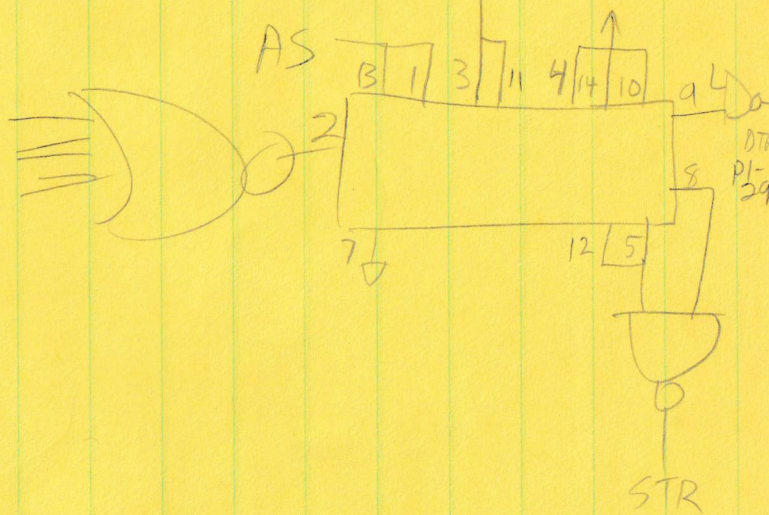
↓  
D0  
D1  
B

D4



CLK PI-70

AS



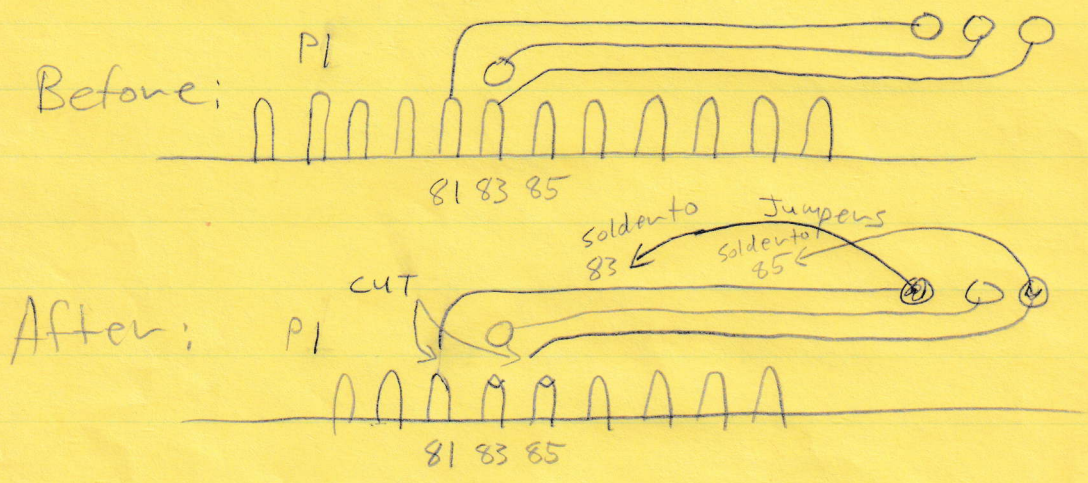
STR



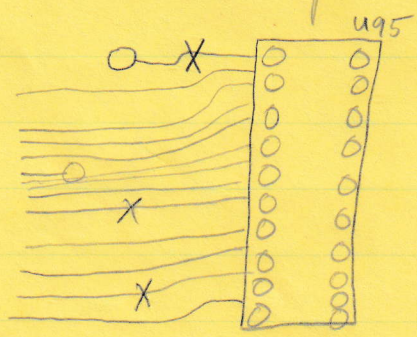
# VTB-102B Mods

★ Problem: AMØ and AM2 signals incorrect at P2.

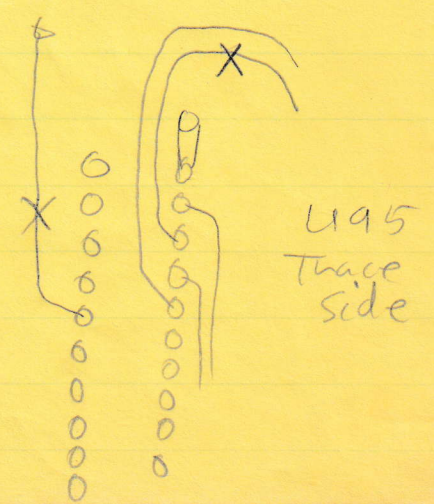
Solution: Cut traces at P2 81 + 83 solder 2 jumpers as shown.



★ Problem: Incorrect traces, U-95  
Solution: Cut traces 5 places, add 1 jumper.  
U 95 component side:



Add jumper, U95 pin 3 to U79 pin 12





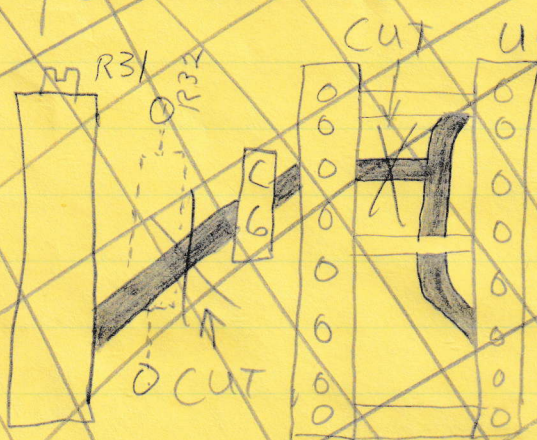
2

Mods, UTB 102B

\* Problem: omitted pullup resistor, U43  
Solution: add 2.2K  $\frac{1}{4}w$  resistor between  
pins 16 + 8 near of board.  
14 Rev

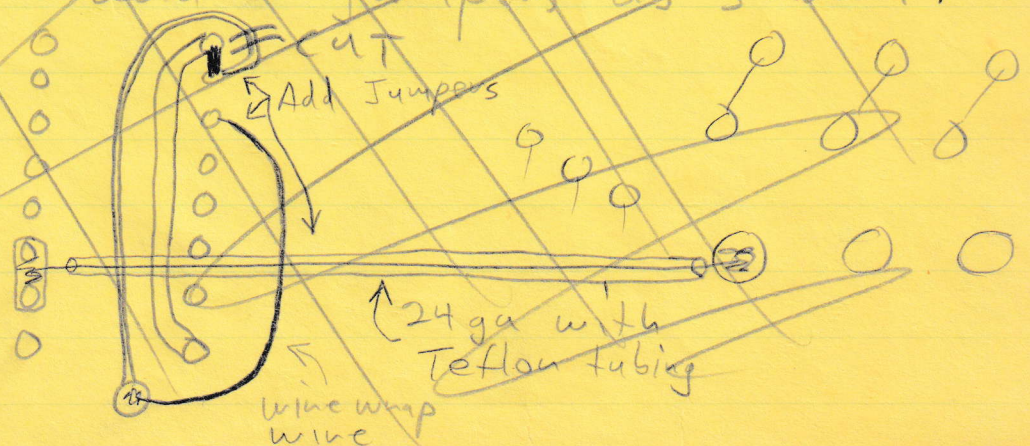
\* Problem: Blank-off led trace omitted.  
Solution: Add jumper, U34 pin 13 to  
U70 pin 11.

Problem: Range of Lores H blanking insufficient  
Solution: Remove U5 from socket,  
remove R32, R33. Cut 2 traces  
component side as shown:



Replace R32  
with a 33K  $\frac{1}{4}w$ .  
Replace R33  
with a 12K  $\frac{1}{4}w$ .

On the rear of the board, cut 1  
trace and add 3 jumpers as shown:





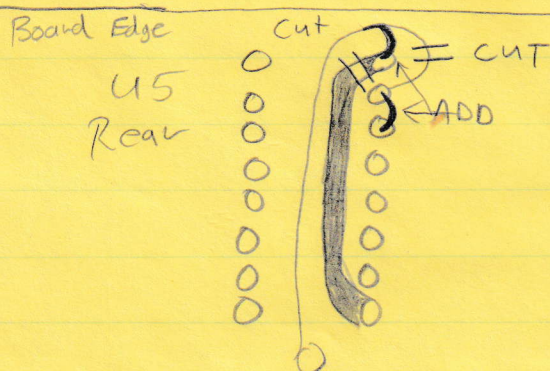
(3)

Mods, UTB 102B

Problem: Lores H blanking range insufficient.

Solution: Replace R 32 with 33K 1/4w 5%.  
Replace R33 with 12K 1/4w 5%.

Cut 2 traces, add 2 jumpers rear side of U5 as shown:



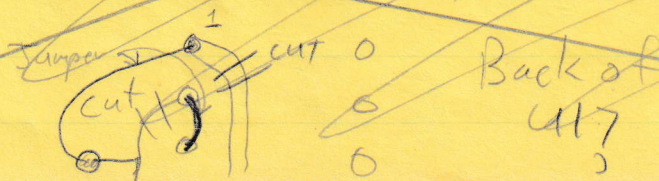
Problem: Lores H clamp<sup>pos.</sup> inadequate range  
Solution: Change R97 to 27K 1/4w 5%

Problem: Hires H blanking<sup>width</sup> inadequate range  
Solution: Change R 56 to 15K 1/4w 5%

Problem: LSYNC and FI TEST traces omitted.  
Solution: Run jumper from U45 pin 2 to U31 pin 20, and from U45 pin 6 to U31 pin 19.

~~Problem: Trigger sense reversed U17~~

~~Solution: cut 2 traces, run 2 jumpers as shown:~~



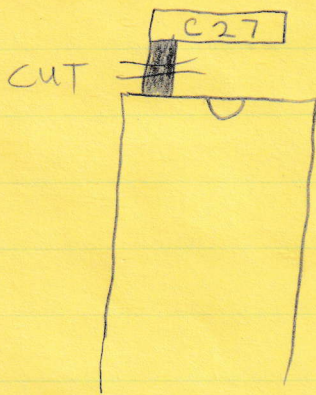


# Problems : UTB102B (4)

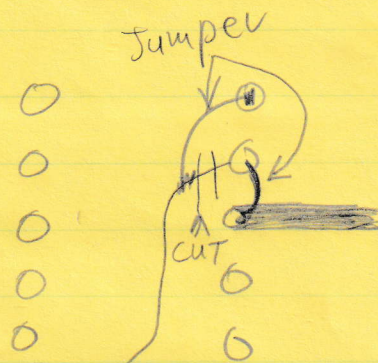
Problem: Trigger sense reversed U17

Solution: cut 2 traces, add 2 jumpers:

U17 Front



U17 Rear



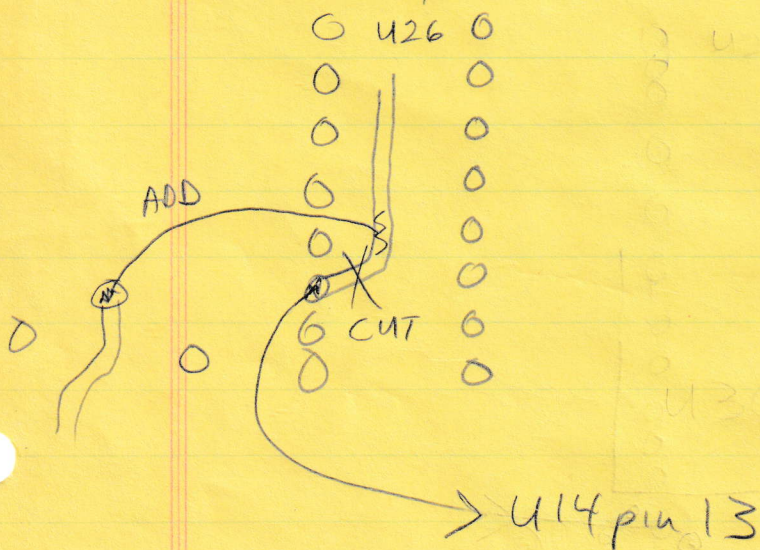
Problem: V blank range inadequate

Solution: Parallel luf across C26,  
change parts list to .22

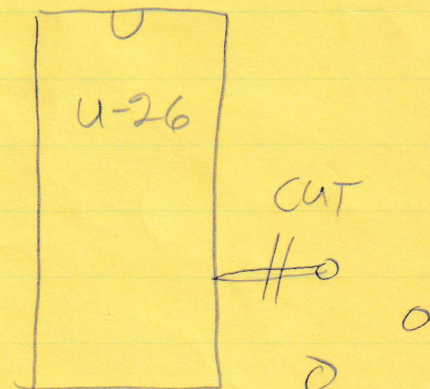
Problem: Change section Reset from  
absolute line # to # lines per section.

Solution: cut 2 traces, add 2 jumpers:

Back,



Front





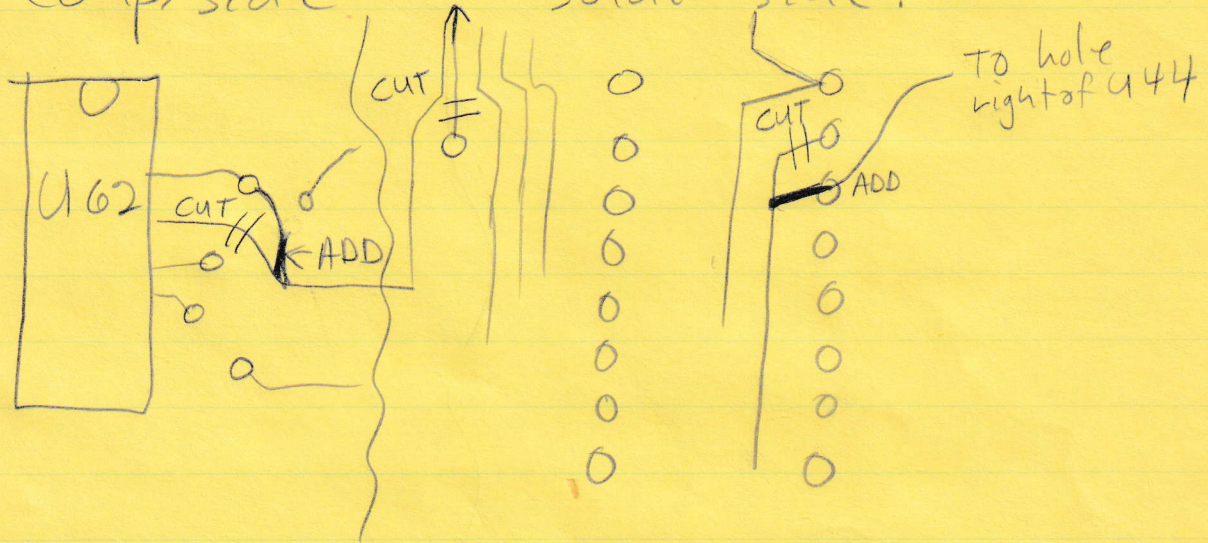
5

Problem: Hires / Norm Vent Reversed

Solution: cut 3 traces, add 3 jumpers:

comp. side

solder side:



Problem: HSRB timing too short

Solution: Replace R48 with 4.7K 1/4w 5%o

Problem: LSRB timing too short

Solution: Replace R49 with 15K 1/4w 5%o

Problem: VR pulse too long

Solution: Replace C17 with .01uf TS cap.

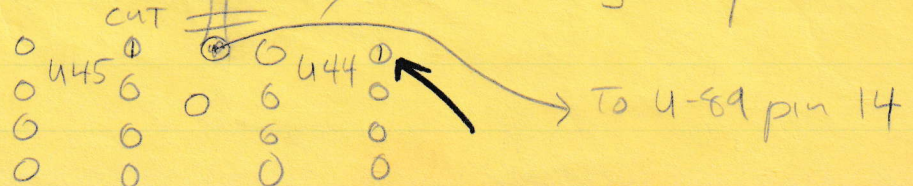
Problem: ZR pulse too short

Solution: Replace R79 with 4.7K 1/4w 5%o

Problem: ZR timing too early

Solution: cut 1 trace, add 1 jumper:

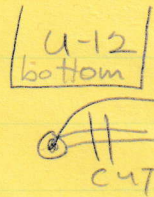
Rear of board:





Problem: Z Ramp FWR blanking incorrect,  
Solution: cut 1 trace, run 1 jumper,

Front  
of Board



Run Jumper on trace side  
to U-62 pin 9.

Problem: Vertical reset not fully discharging  
C117.

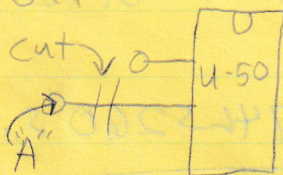
Solution: Jumper U-84 pin 9 to 13,  
pin 1 to 7, pin 14 to 8, (parallel switches)

Problem: Test switcher, trace omitted, <sup>CRT</sup> Blanking  
Solution: Add 1 jumper, U31 pin 2 to U70 pin 6

Problem: Disabled Z Ramp oscillates

Solution: cut 1 trace, add 3 Jumpers, <sup>1 Resistor</sup>

Front



Jumper from hole "A" to  
U-33 pin 11. Jumper from  
U-33 pin 12 to U-52 pin 4.

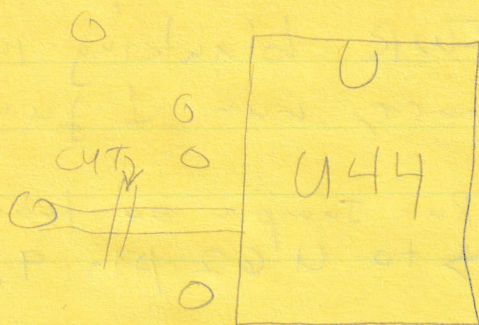
Install 270Ω Res. U-34 pin 2 to U-52 pin 3,  
Jumper U-34 pin 2 to U-33 pin 13, and U-34 pin 1 to U-62 pin 9

Problem: LHC clamps wrong during vertical  
Solution: cut U20 pins 10 + 11 free (near of board)  
add jumper to U17 pin 12,

Problem: V+H Blanking comparators oscillate,  
Solution: Put 27KΩ 1/4w 270 in parallel with  
5pF caps between pins 3+11 of U 72, 73, 21, 35,  
ALSO U3, U11.



Change C1 from 1uf to 10uf



Solution:

Change C81 to 56 pf

Swap C83 for 470  $\Omega$

Problem:

Z Ramp Range

Problem: Z Reset left off

Solution: Cut trace from 13 of U52 to 15 of U71

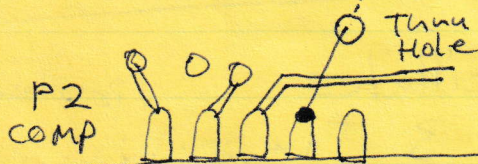
Jumper from U33 pin 11 to 15 of U71

Solution:

Wire from U62 pin 9 to U43 pins 1+2.

Wire from U43 pin 3 to P2-93 (comp side)

Problem: white pulse left off board



Problem: Intermittent glitches out of U96 due to Data Strobe undershoot.

Solution: use ONLY motorola 74LS260's in U96.

~~use 74LS260 in U96~~

Problem: Blanking Bas not sufficiently driven by LS260.

Solution: Use 74LS260 in U70. Change Parts list.

Problem: COHA Ant cam won't tolerate Hi/Lo Res switching.

Solution: make it always get lines reset by cutting trace going to pin 8 of U91.

(comp side) Jumper 8 of U91 to pin 5 of U62



# VTB MODS

(7)

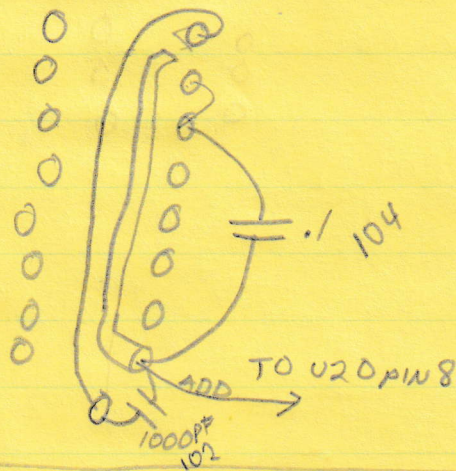
Problem: GLITCH

Solution: U5 ADD 2 CAPACITORS, add 1 JUMPER

.1uf BETWEEN PIN 3 and PIN 8

1000pF BETWEEN PIN 8 and CLOSEST HOLE TO LEFT

JUMPER U5 PIN 8 TO U20 PIN 8



ADD JUMPER FROM U17 PIN 13 TO U46 PIN 11

ADD JUMPER FROM P1- TO U90 PIN 8 TO U63 PIN 8 TO  
U44 PIN 8 TO U27 PIN 8 TO U18 PIN 8 TO

C30 - .1uf ABOVE U18



CUT TRACE BETWEEN JUMPER J2



user ~~1004~~  
VAO 100A.FX

VAO Fixes:

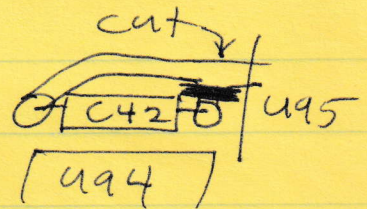
IMPORTANT !!!

Must be done before  
Firing up VAO-100A

Problem: P1 +5 and GND connected by ACS.

Solution: Cut between Pin 1+3 comp side P1,  
also cut <sup>near</sup> C42 legend as shown:

Problem: -15 connected to pin 7  
of U32 +34.



Solution: cut old connection to pin 7,  
Jumper <sup>pin</sup> to pin 10, both IC's

Problem: Spare decoder enabled instead of  
oscillator 3+4,

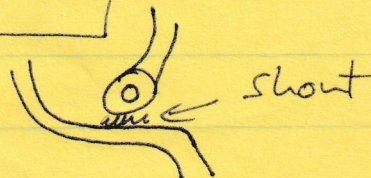
Solution: Re-burn ~~U-77~~ PROM U-77

Problem: C15 and C12 stuffed with 1000 instead  
of 100pf. Solution: replace with 100pf.

Problem: short on board near bottom U58

Solution: EXACTO!

U58



NOTE:

ON REV  
A boards,  
Parallel 1000pf  
from above  
with existing  
1000 pf

Problem: Range of HFOSC

Solution: Change values: R14, R15 = 3.9K

C11, C16 = 2,000pf



VAD page 2

INVERT BITS 4 + 12 to Max Regs

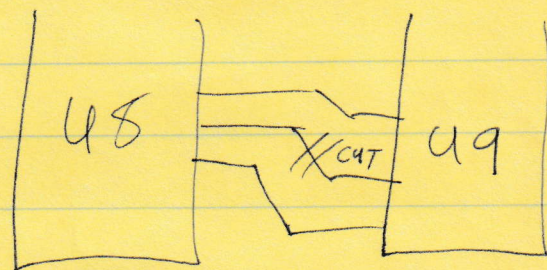
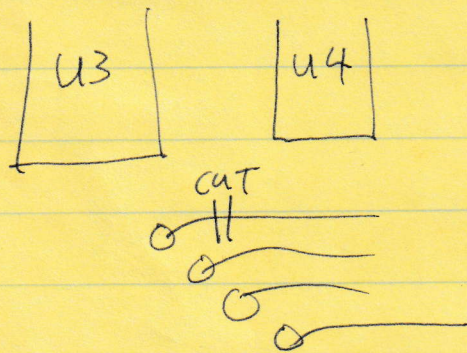
MAKE 2 CUTS BY U4 + U8

JUMPER U91-5 to U81-3

JUMPER U81-4 to U7-8

JUMPER U92-5 to U81-9

JUMPER U81-8 to U8-8



COMP. SIDE

Change R51 and R33 to 3.32 k

JUMPER

U64-1 TO U77-6

U64-2 TO U29-6

U64-3 TO U29-8

PCS forgot

carry in was tied to +5 not GND

cut trace U37-7

JUMPER U37-7 to U37-8

JUMPER U20, U21, U22 PINS 1-28

U20-1 TO U20-28

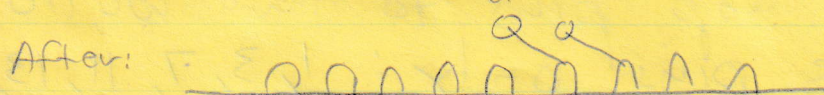
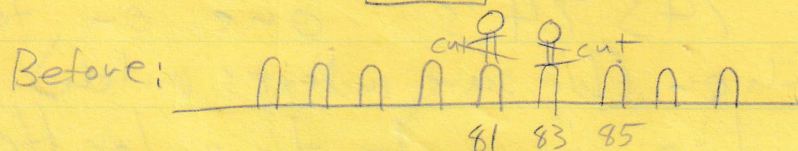
45-48 pins LOW FREQ. TRNG  
5-40ms HIGH " TRNG



①

## VCB-101A Mods

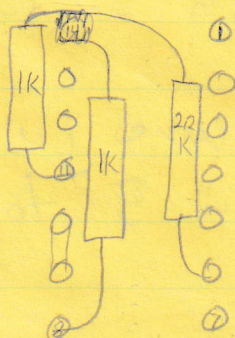
- Problem: Address modification bits incorrect
- Solution: Cut 2 traces, add 2 jumpers:



- Problem: U-128 pullup resistors omitted,

Solution: Add 2.2K  $\frac{1}{4}w$  5% from U-128 pin 6 to 14;  
Add 1K  $\frac{1}{4}w$  5% from U-128 pin 8 to 14; Add 1K  $\frac{1}{4}w$  5% from U-128 pin 11 to 14 as shown;

U128 Rear:



- Problem: Inadequate bias, RGB in amps,

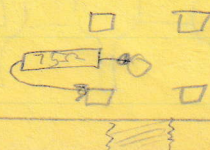
Solution: Replace R585, 416, 399 with 910  $\Omega$   $\frac{1}{4}w$  5%

- Problem: RGB inputs drift during vent int,

Solution: Remove R267, 361, 376

- Problem: RGB inputs not terminated

Solution: add 75  $\Omega$  resistors, back of RGB in connectors:



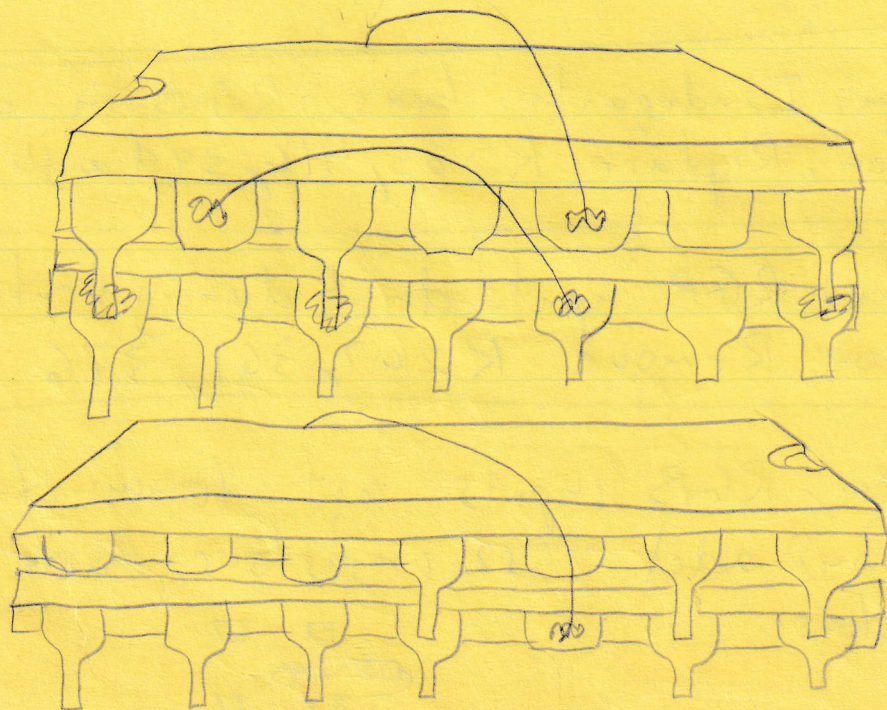


UCB 101A Mods

(1a)

## 74S74 piggyback for U-125

- Stack two 74S74's. one on top of the other. (be sure indexes match)
- Solder the top pins to the bottom for these pins only: 1, 3, 7, 11, 13, 14.
- Cut the pin part of the leg off for the top chip's pins 2, 4, 5, 6, 8, 9, 10, 12.
- Cut the pin part of the bottom chip's leg at pin 12.
- Solder a wirewrap wire jumper from the bottom chip's pin 5 to the top chip's pin 2.
- Solder a wirewrap wire jumper from the top chip's pin 5 to the bottom chip's pin 12.





## UCB101A Mods

(2)

~~Problem: Over-bias of output buses~~

~~Solution: Jumper between the following:~~

~~U6 - pin 5 to 6, U23, pin 5 to 6, 9 to 10~~

~~U31 pin 5 to 6, 9 to 10, U55 pin 5 to 6, 9 to 10~~

~~U63 pin 5 to 6, 9 to 10.~~

Problem:  $\pm 15$  traces left off, U33.

Solution: Jumper U33 pin 11 to U16 pin 11  
and U33 pin 12 to U16 pin 12.



VCB 101

Colonizer

Problem: Resistor Value Change

Solution: Remove  $15K\Omega$ : R83, 88, 92, 96,  
100, 149, 154, 158, 162, 166, 211, 216, 220, 224, 228.

Replace with  $6.81K \frac{1}{4}w 1\%$ .

---

Remove  $6.8K$ : R82, 87, 91, 95, 99, 148, 153,  
157, 161, 165, 210, 215, 219, 223, 227

Replace with  $3.32K \frac{1}{4}w 1\%$ .

---

Remove  $430\Omega$ : R71, 107, 106, 141, 175, 174,  
200, 238, 237, 263, 282, 281, 309, 330, 329,  
357, 396, 395. Replace with  $200\Omega \frac{1}{4}w 1\%$

---

Remove  $56p$ : C17, 22, 21, 23, 26, 25, 27, 32, 31,  
33, 38, 37, 39, 42, 41, 43, 47, 46.

Replace with  $220pf$

---



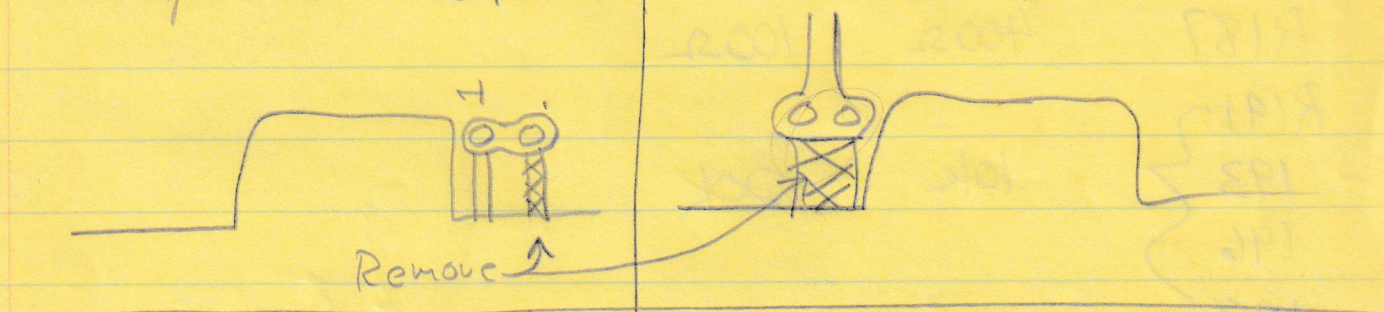
## VID Connections:

Problem: PCS misconnected +5 to GND,

Solution: Cut Fingers off!!!

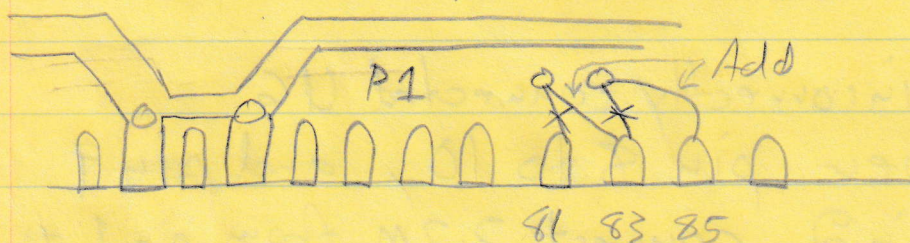
Component side:

Trace side:



Problem: Address modifier bits swapped

Sol: cut 2, Jump 2: component side



Problem: R66 connected to gnd, instead of 5

Solution: Remove R66, scrape gnd from comp side:

Replace R66 with  $475\Omega$ , jumper bottom R66 to bottom R56.

Problem: R48 inadeg range Solution: Replace R64 with  $3.0\Omega$

Problem: Clamp errors, Solution: add

-200K, near of board from bottom R90 to top R91

-360K, " " bottom R94 to top R91.



Problem: Grey level ref voltage change

Solution: Resistor value changes as follows:

Part	was	now
R184	1.6K	2.0K
R185	400 $\Omega$	Jumper
R186	1.6K	2.0K
R187	400 $\Omega$	100 $\Omega$
R191	10K	20K
193		
196		
198		
R279	2.2K	470 $\Omega$
R50	680 $\Omega$	322 $\Omega$

Problem: PCS incorrectly connected U6

Solution: jumper pin 8 to 10, and pin 9 to U42 pin 2, connect 2.2M from pin 1 to +15V.

Problem: Response + Ampl of Grey levels

Solution: replace C7 with 220pf put 24 $\Omega$  resistor between TP-5 and ground.

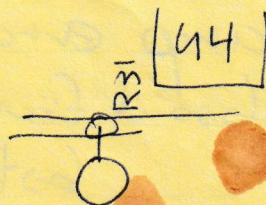
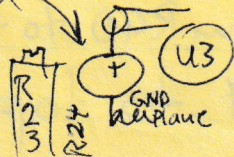
Problem: Wrong resistor installed in R28 (470 $\Omega$ )

Solution: Should be ~~470 $\Omega$~~  51 $\Omega$

Problem: Inadeq bypass, video multiplier.

Solution: Install 1 $\mu$ f near R31 symbol and near R24 symbol

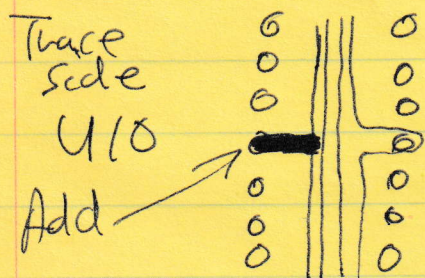
Add





Problem: PCS omitted -15 to U10

Solution: Connect as follows

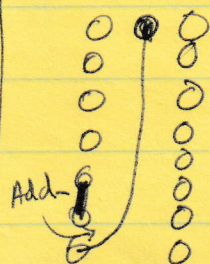
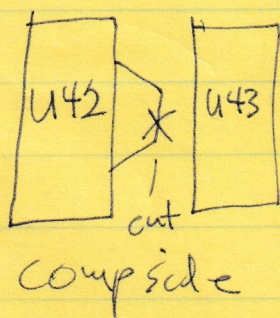


Problem: Analog and Encode bits swapped (PCS)

Solution: Table change in software

Problem: Sense of HB inverted.

Solution: Cut trace between U42 + U43 <sup>component side.</sup>  
Add trace from U42 pin 9+10, and from



U42 pin 8 to pad  
near pin 13 (Trace side)

Trace side

Prob: -15 left off U22, Sol: Jump from U-21

Prob: Clamp errors: Solution change R162 + R173 to  
~~10002~~ 680  $\Omega$

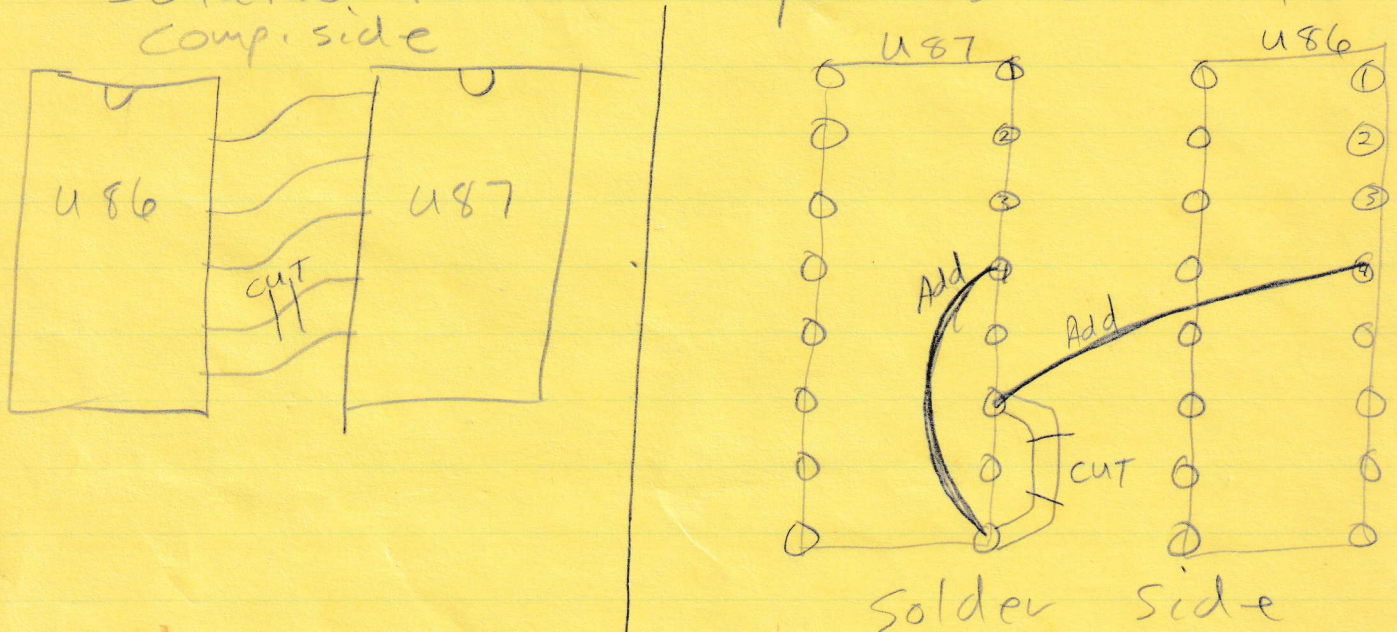


1

# URM Fixes:

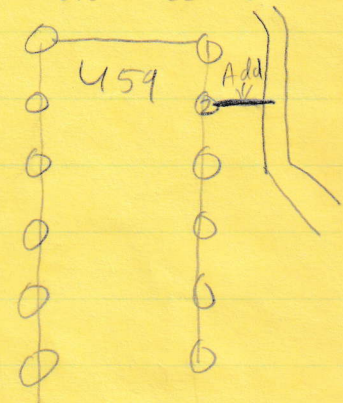
Problem: U87 pins 4 and 6 swapped.

Solution: Cut + Jumper as shown comp. side



Problem: U59 pin 2 ground, not connected.

Solution: connect!



Problem: Value changes:

- Change R68, 61, 53, 76 from 100K $\Omega$  to 100 $\Omega$ .
- change R80, 81 from 10K $\Omega$  to 6.8K $\Omega$

Problem: Noise - Solution: Jumper between P1 pin 3 and Ground plane area above P2-119



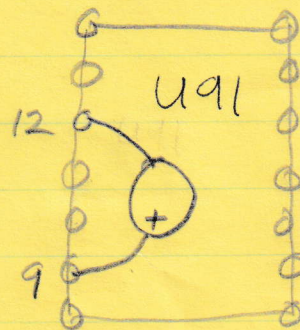
# VCR MODS -

- Problem - Dac Zero Inadeq Range  
 Solution - Replace ALL 2.2M with 100k,  
 R5, 8, 11, 14, 32 - 38, 49

- Problem - Perspective divider adjust  
 Inadeq Range  
 Solution - Replace R67 with 5.1K  
 Replace R70 with 10K

- Problem - PCS neglected note 5 on schematic  
 Solution - short pin 18+19 together  
 on ~~U8, U3, U7, U4, U6, U5~~  
 U3 thru U8

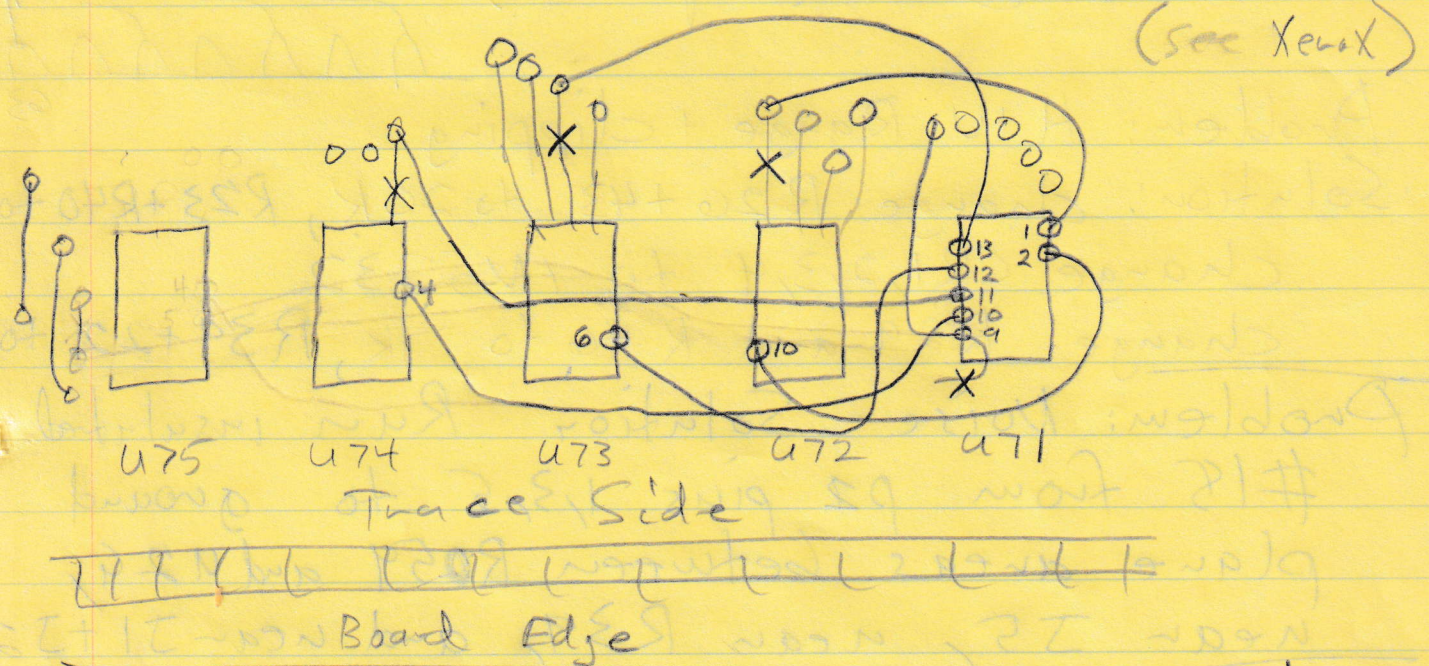
- Problem - PCS left off  $\pm 15V$  bypass caps  
 U90-93, Fix: Comp side = add 1uf  
 cap: solder to ground plane | trace side: 1uf cap:



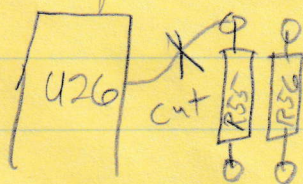


# VCR Mods p2

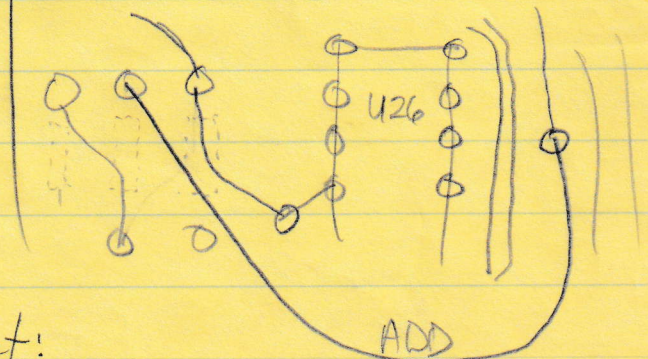
Problem: Data inverted to Analog Mux's  
 solution: Replace U76+78 with 74LS244,  
 cut 4 places, add 7 jumpers as shown!



Problem: Input to U26+27 connected  
 by PCS - to pin 11 of U26 (WRONG!)  
 Solution: 1 cut, 1 jumper as shown!  
 Comp side:



Trace side:



Problem: Intensity Offset:

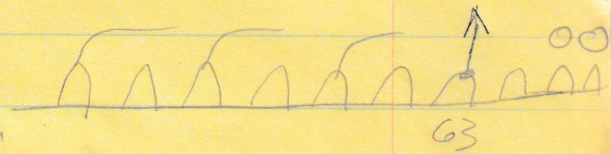
Solution: Change R53 to 20K, Add 62K from U23  
 pin 2 to pin 4



~~POT~~ ~~R39 277 $\Omega$~~   
~~R22 320 $\Omega$~~

Problem: Divider output left off board.

Solution: add jumper from bottom of J4  
to P2-63 (comp side)



Problem: H+V Range + Clipping

Solution: change R26+43 to 20K, R23+R40 to 5.1K

change CR1,2,3,4 to 1N5232

change R29 and R46 to 1K, R39+22 to 200 $\Omega$

Problem: Noise - Solution Run insulated  
#18 from p2 pins 1,3,5 to ground  
plane areas between R59 and U24,  
near J5, near R39, and near J1+J2.

Problem: 2 blanking range - solution: change  
R57 to 20K, connect to -15 instead  
of ground.



## VRG FIXES

P1

Problem: LH0062 -15 connected to pin 4 instead of pin 5

Solution: cut -15 to pin 4, jumper to pin 5 for U1, 2, 22, 3, 4, 24  
5, 6, 26

---

Change Address Modifiers as on VCB

---

Add 1K pullup U113-pin 3 to +5

---

Change DAC Trimmers to 100K

---

U86 pin 3 not connected.

---

change R 21 from 68K to 33K

R 4 from 180K to 150K

R 6+23 from 10K to 5K

R 5+22 from 20K to 10K

---

Change U-100 + U-102 to 74LS244

---

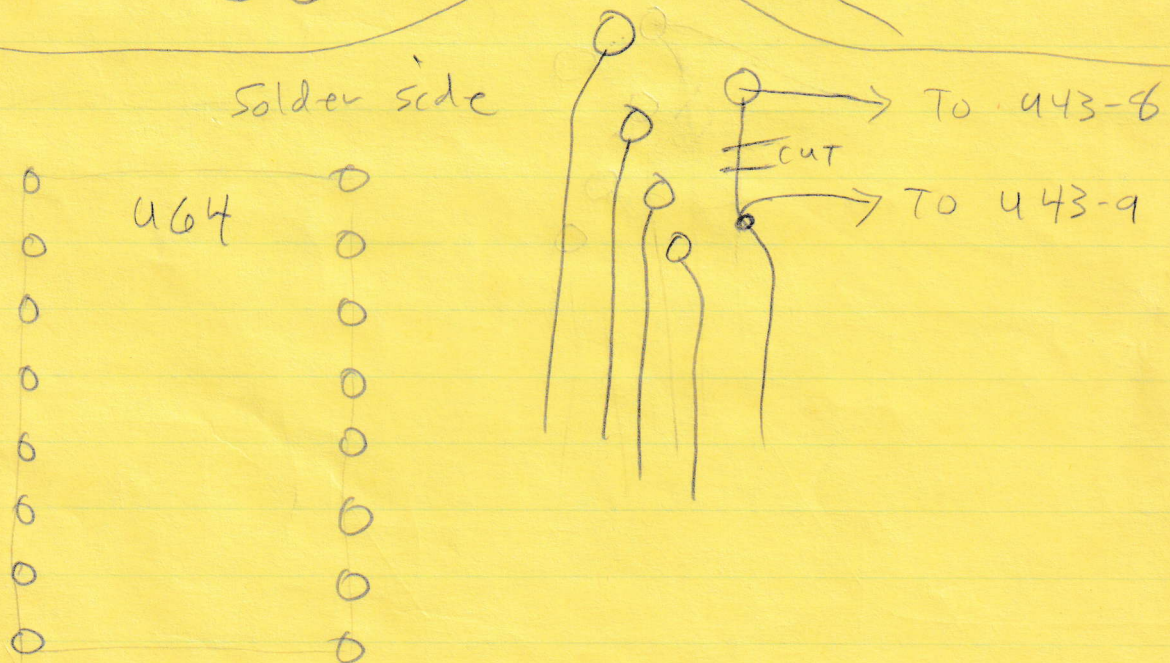
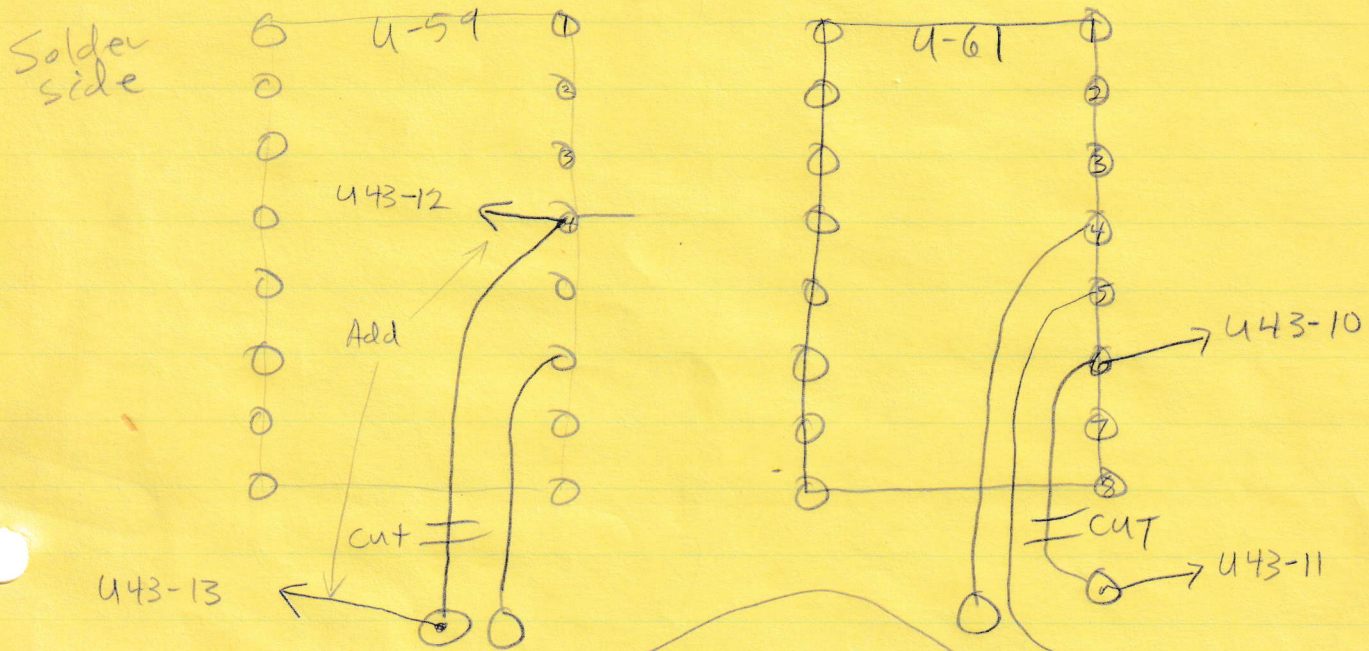
U-21 pin 7 not grounded. Run from pin 8



# VRG Fixes p 2

Max Data Invented: change U-100, 102 to 74LS244,

Problem: Invent bits 4, 9, 14 to Analog Muxes. with spare inv in U-43  
Fix: 3 cuts, 6 jumpers as shown:





# VRG Fixes P 3

Problem: Intensity parameters from Size, Axis to P-2 left off board.

Fix: Add 3 wires as shown:

- from U-22 pin 8 to P2-18
- from U-24 pin 8 to P2-34
- from U-26 pin 8 to P2-36

SOLDER SIDE, P2 (RIGHT)



★ Problem: Noise

Solution change C 1, 4, 5, 7, 9, 12, 13, 15, 17, 18, 19, 20, 21 to 15pf, add .1 bypass  $\pm 15$  to U 15, 17, 19.

★ Run #18 insulated wire from P2 pins 1, 3, 5 to Ground plane area ~~area~~ between U15 + U16.



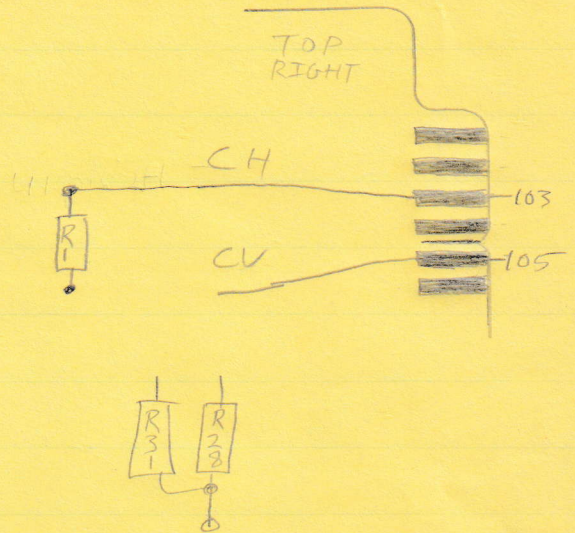
User 1106

COHU IFX

# COHU ART CAM MODS

## - DEFL BD

- \* Edge conn #103 to Top of R1.
- \* Lift bottom of R31, connect to bottom of R28:

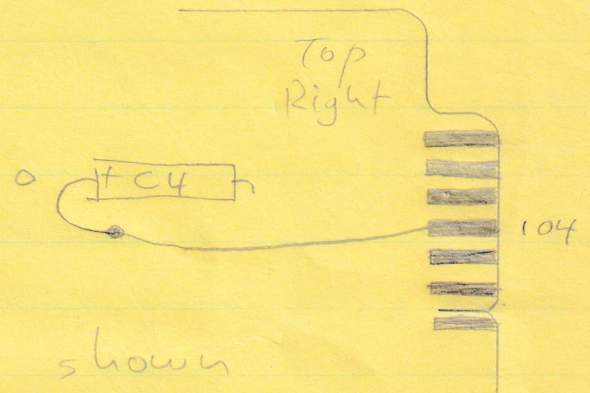


- \* Remove E2 near TP2
- \* Edge connector 105 to C2 hole near TP2

- \* Add Red MOD sticker

## - Blanking BD

- \* Lift + side of C4
- \* Edge connector #104 to + side C4
- \* Add MOD sticker



## - Frame: Add wires as shown

J4	
101	1
102	2
103	3
104	4
105	5
106	6
107	7

J3	
101	1
102	2
103	3
104	4
105	5
106	6
107	7

CH

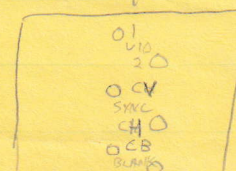
CV

J2	
101	1
102	2
103	3
104	4
105	5
106	6
107	7

J1	
101	1
102	2
103	3
104	4
105	5
106	6
107	7

## - Back Panel CB

- \* disconnect loop thru and coaxes to bottom 4 connectors.
- Re-label



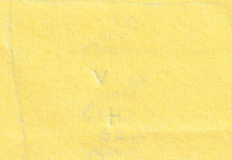
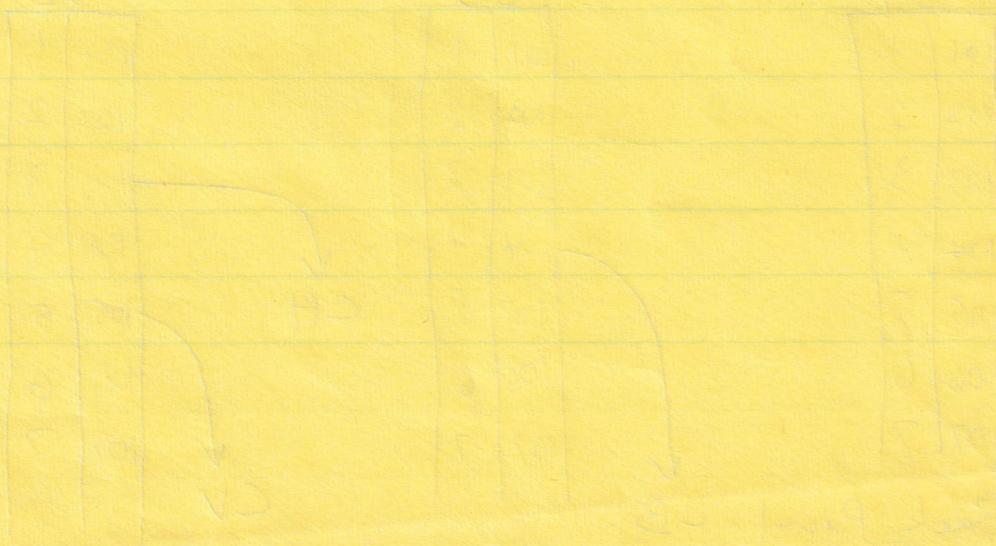
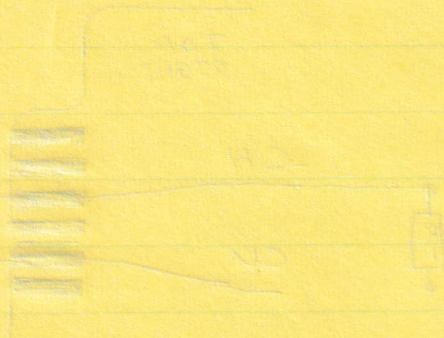
Back view



231 - R 207

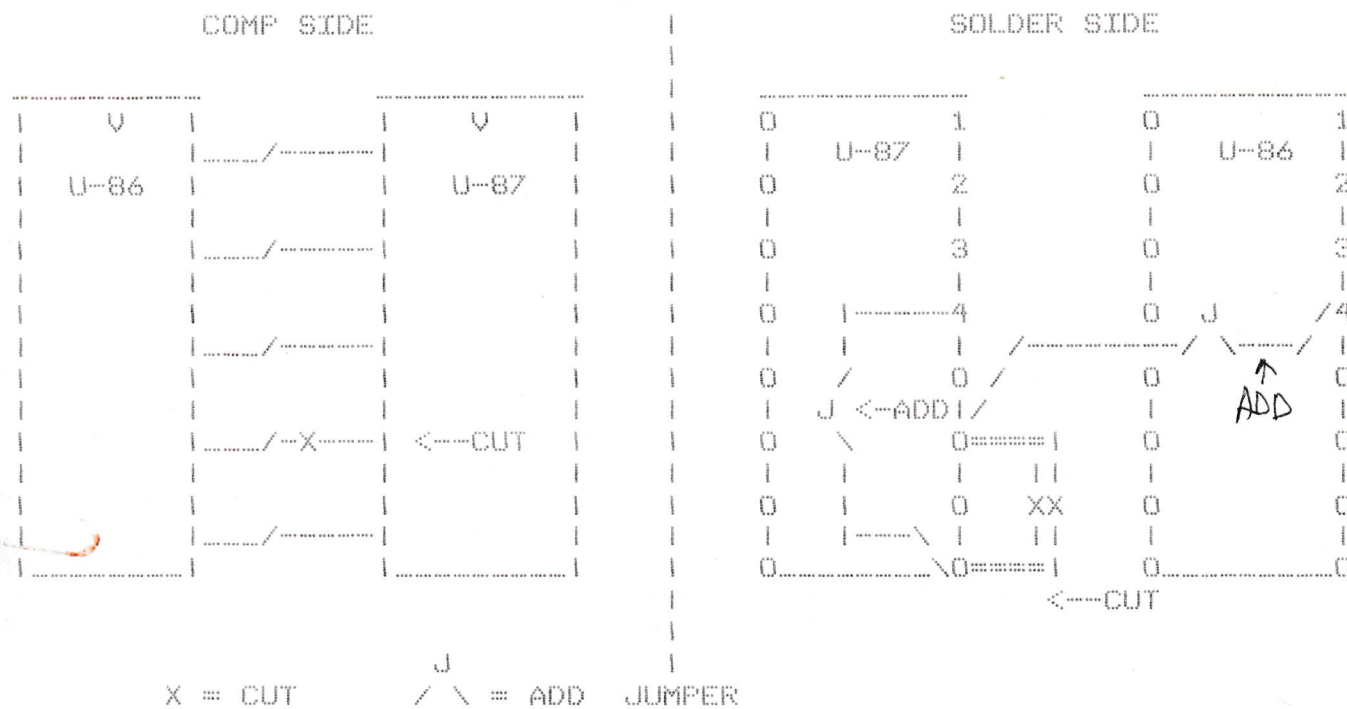
2011 1102

R 34 45 60 61 AD TSA

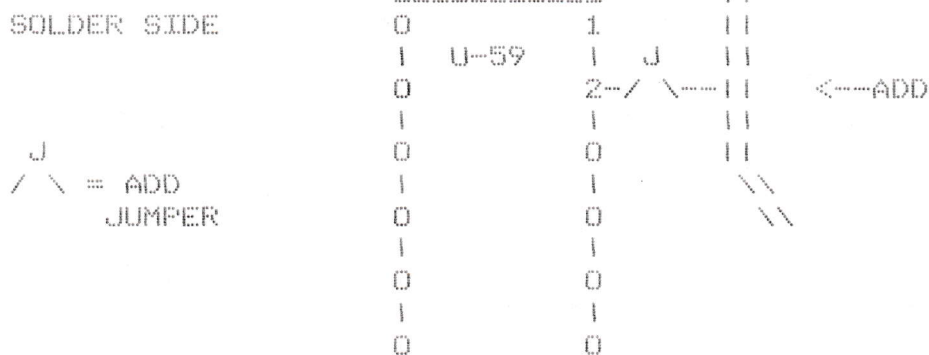




SOLUTION: CUT AND JUMPER AS SHOWN:



SOLUTION:      CONNECT:





\*PROBLEM: VALUE CHANGES.

SOLUTION: CHANGE R68, 61, 53, 76 FROM 100K ohms TO 100 ohms.  
---CHANGE R80, 81 FROM 10K ohms TO 6.8K ohms.

\*PROBLEM: NOISE.

SOLUTION: JUMPER BETWEEN P1 PIN 3 AND GROUND PLANE AREA ABOVE P2 - ~~11~~  
119



VRG FIXES

\*PROBLEM: LH0062 -15 CONNECTED TO PIN 4 INSTEAD OF PIN 5.

SOLUTION: CUT -15 TO PIN 4, JUMPER TO PIN 5 FOR U-1, 2, 22, 3, 4, 24, 5, 6, 26

---CHANGE ADDRESS MODIFIER AS ON VCB.

---ADD 1K PULLUP U-113 PIN 3 TO +5.

---CHANGE DAC TRIMMERS TO 100K.

---U-86 PIN 3 NOT CONNECTED.

---CHANGE R-21 FROM 68K TO 33K;

R-4 FROM 180L TO 150K;

R-6 + 23 FROM 10K TO 5K;

R-5 + 22 FROM 20K TO 10K.

---CHANGE U-100 + U-102 TO 74LS244.

---U-21 PIN 7 NOT GROUNDED. RUN FROM PIN 8.

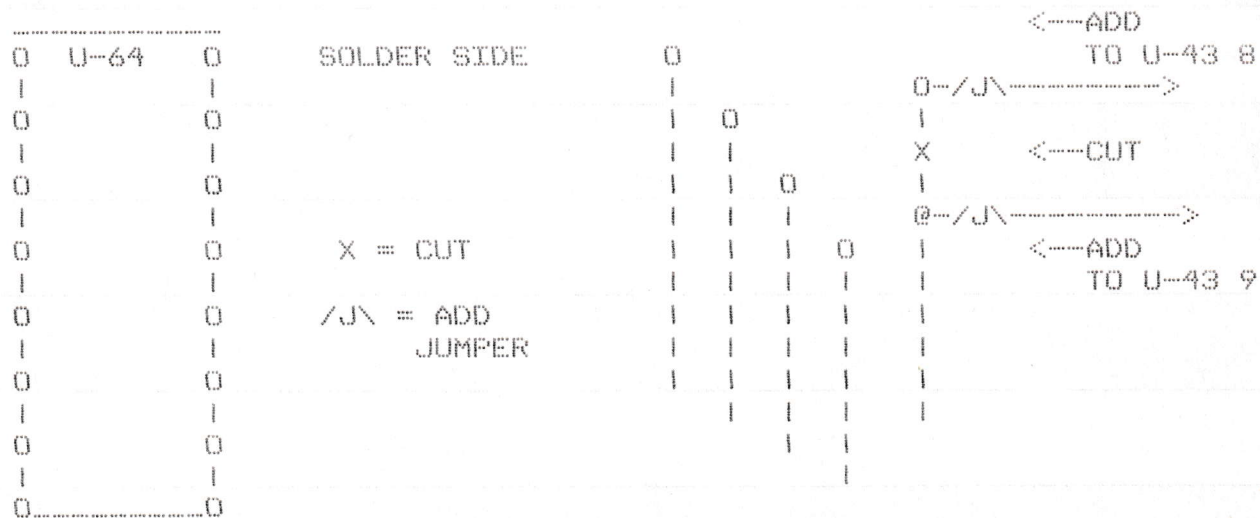
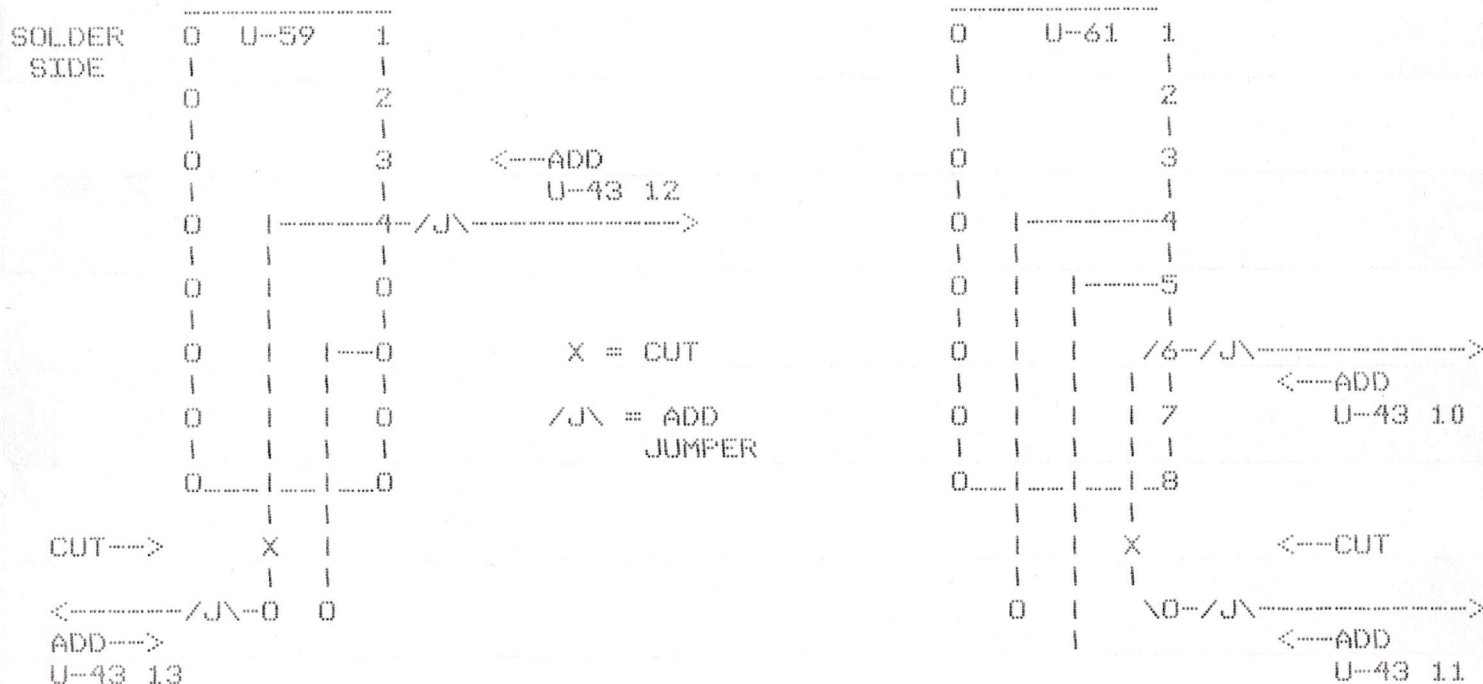


```
*PROBLEM:  MAX DATA INVERTED.
```

SOLUTION: CHANGE U-100, 102 TO 74LS244.

---INVERT BITS 4, 9, 14 TO ANALOG MUXES WITH SPARE IN U-43.

---3 CUTS, 6 JUMPERS AS SHOWN:

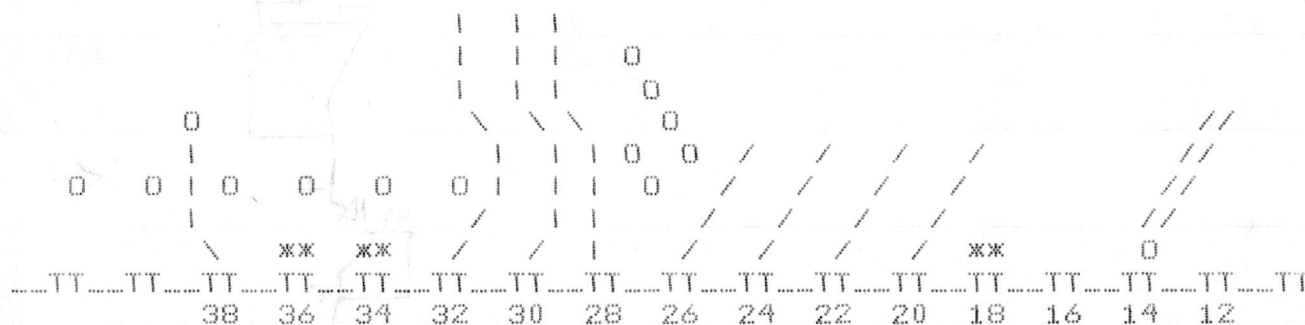




\*PROBLEM: INTENSITY PARAMETERS FROM SIZE, AXIS TO P2 LEFT OFF BOARD.

SOLUTION: ADD 3 WIRES AS SHOWN (\*\*):  
 --FROM U-22 PIN 8 TO P2 - 18;  
 --FROM U-24 PIN 8 TO P2 - 34;  
 --FROM U-26 PIN 8 TO P2 - 36.

SOLDER SIDE, P2 (RIGHT)



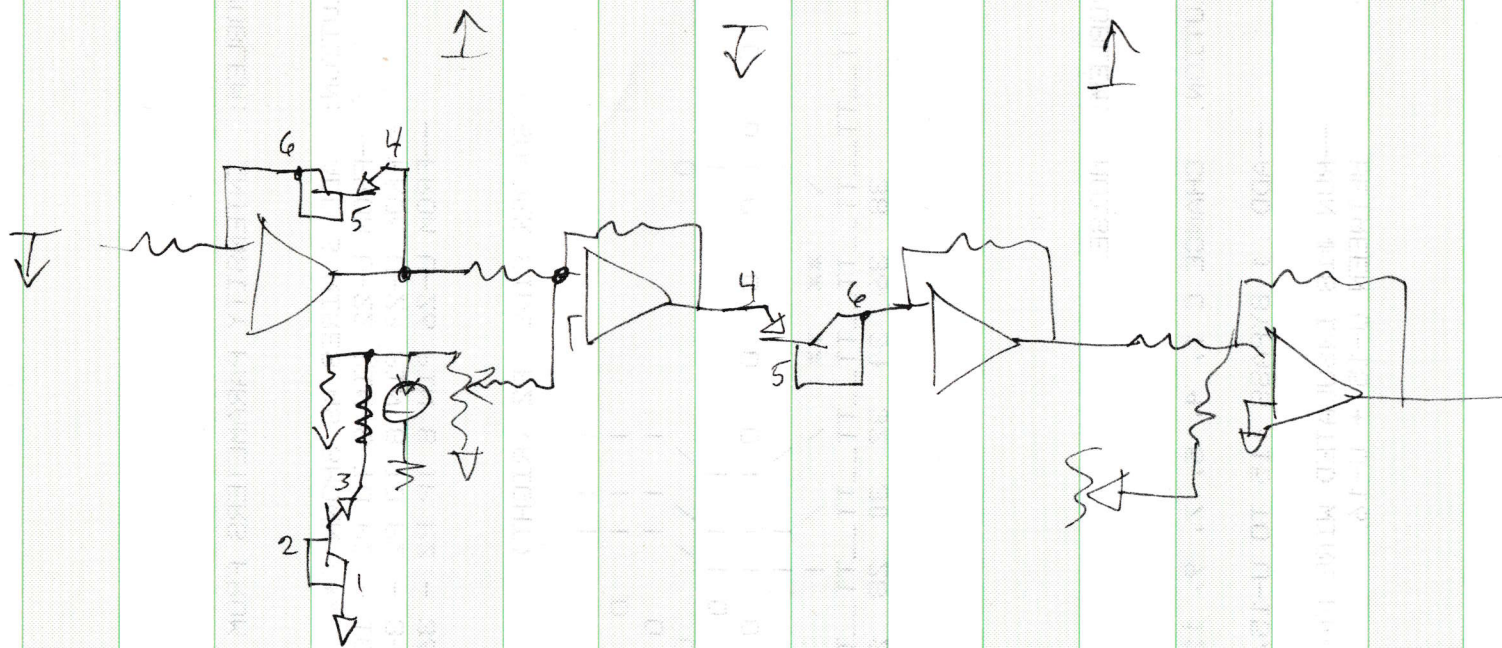
\*PROBLEM: NOISE.

SOLUTION: CHANGE C 1, 4, 5, 7, 9, 12, 13, 15, 17, 18, 19, 20, 21 TO 15pf;  
 --ADD .1 BYPASS +15 TO U-15, 17, 19;  
 --RUN #18 INSULATED WIRE FROM P2 PINS 1, 3, 5 TO GROUND PLANE AREA BETWEEN U-15 + U-16.

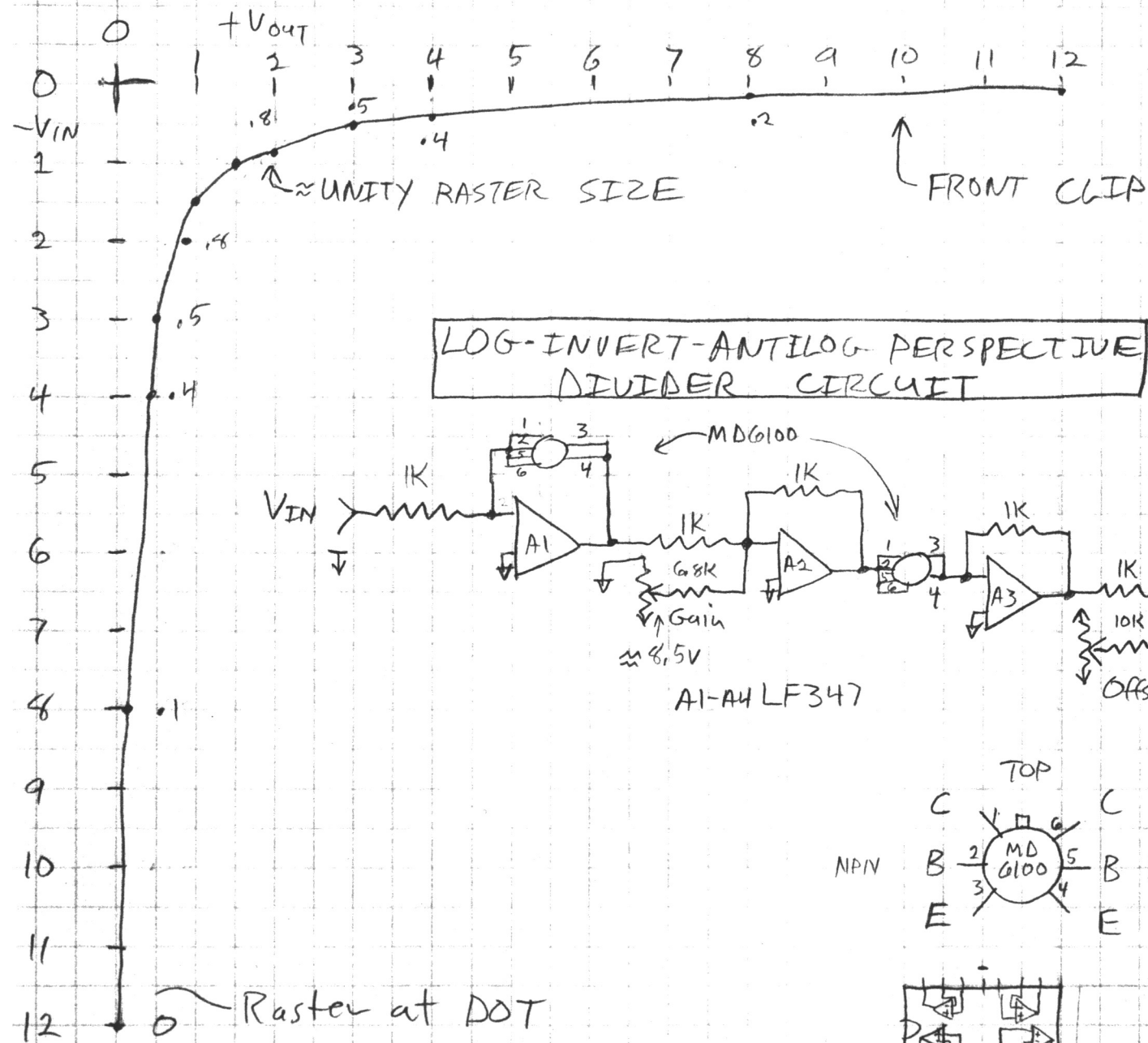
\*PROBLEM: PIN 4 CONNECTED TO -15.

SOLUTION: CHANGE -15 TO PIN 5.

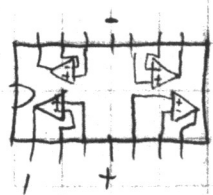
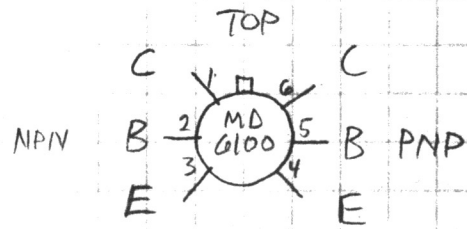
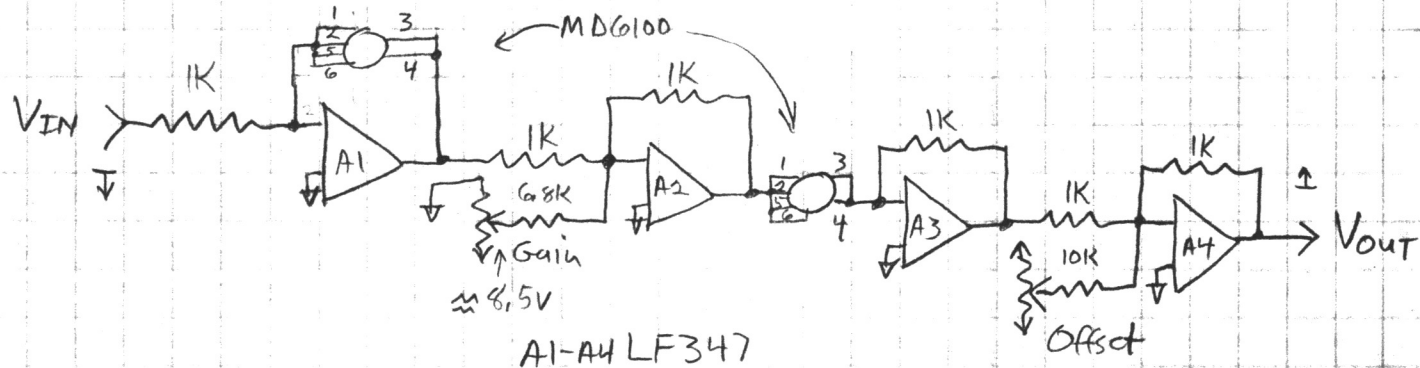








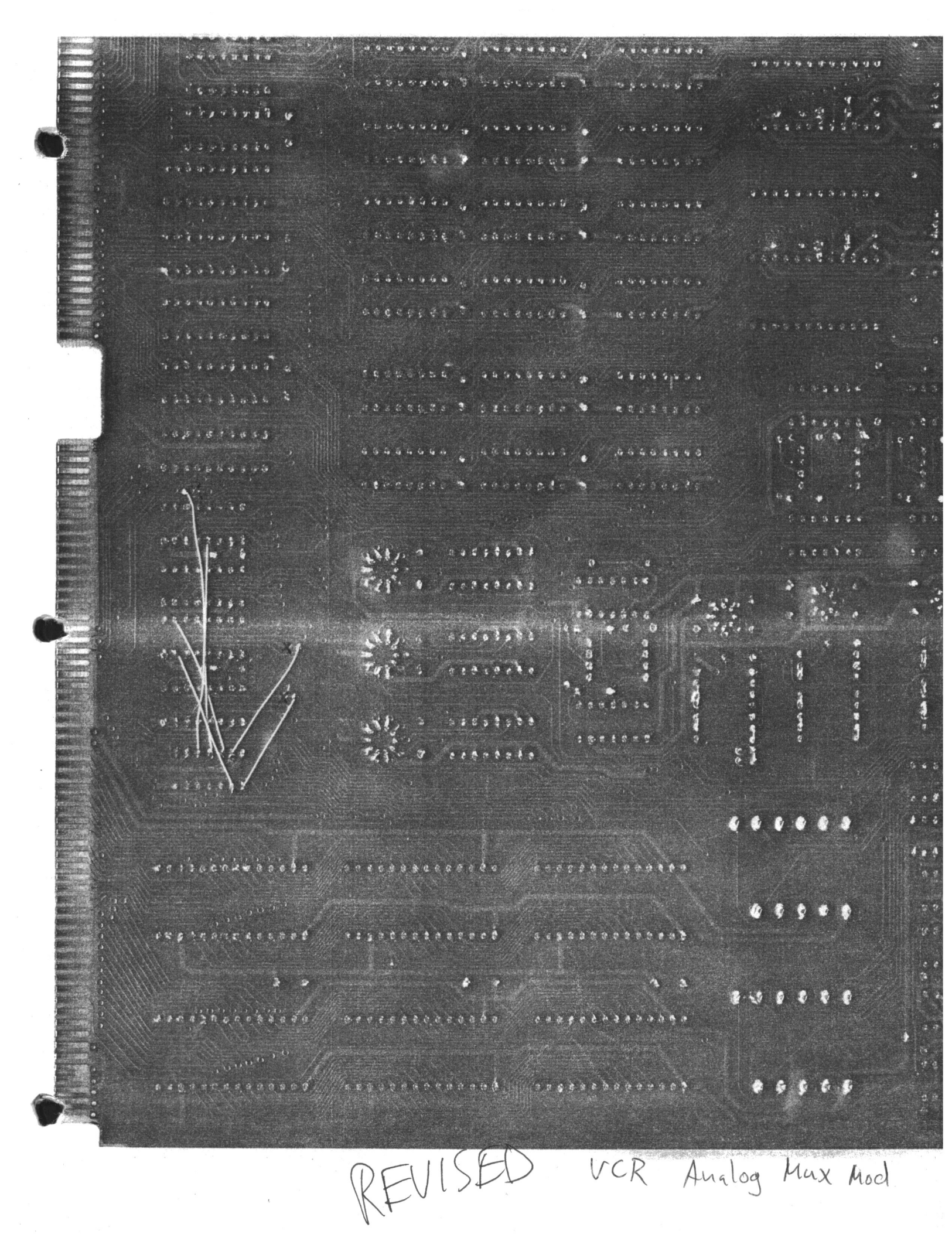
# LOG-INVERT-ANTILOG-PERSPECTIVE DIVIDER CIRCUIT



Raster at DOT  
Adjust with offset pot  
for Zero Out.

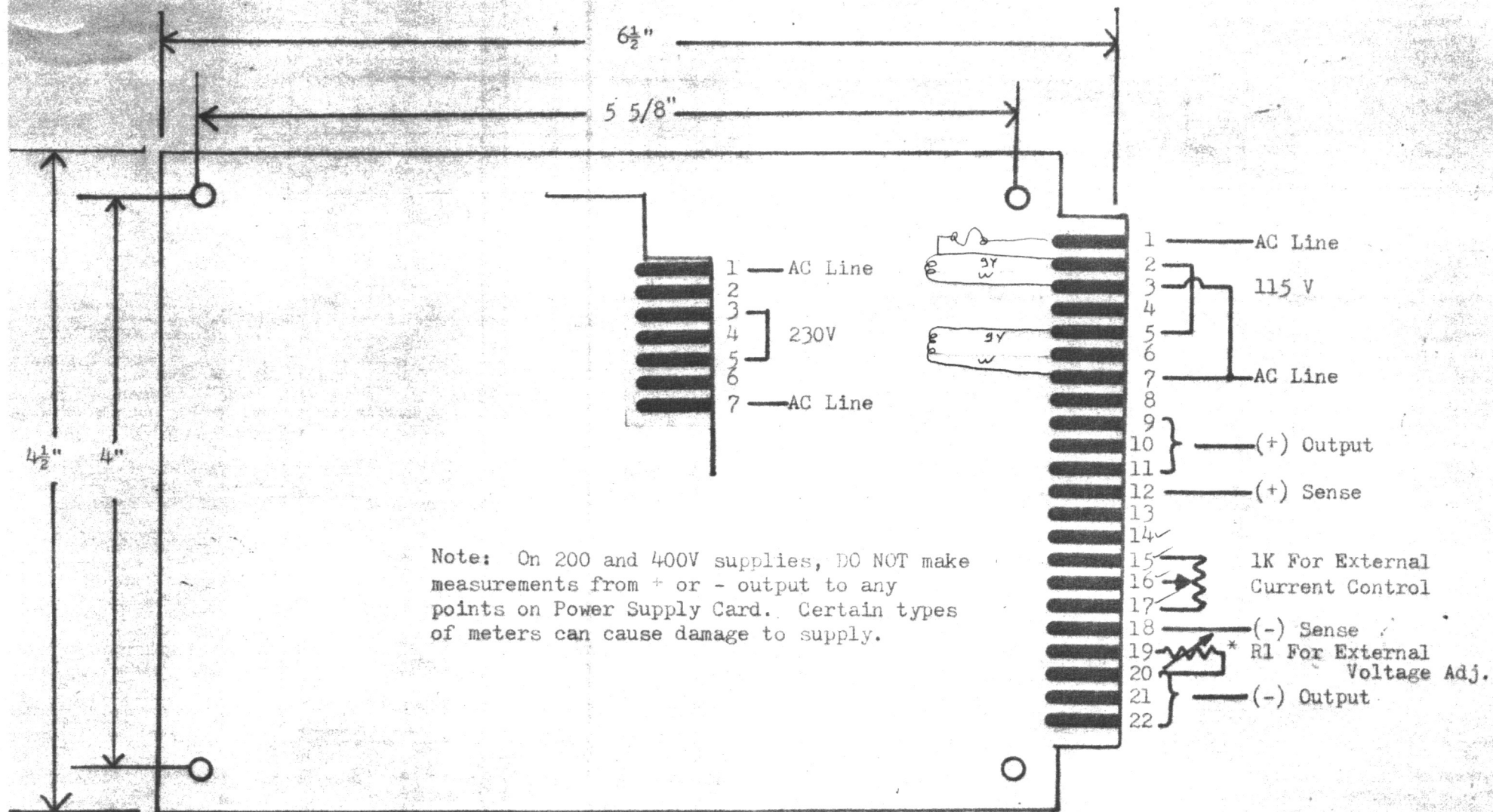
4/81 DWS





REVISED VCR Analog Max Mod





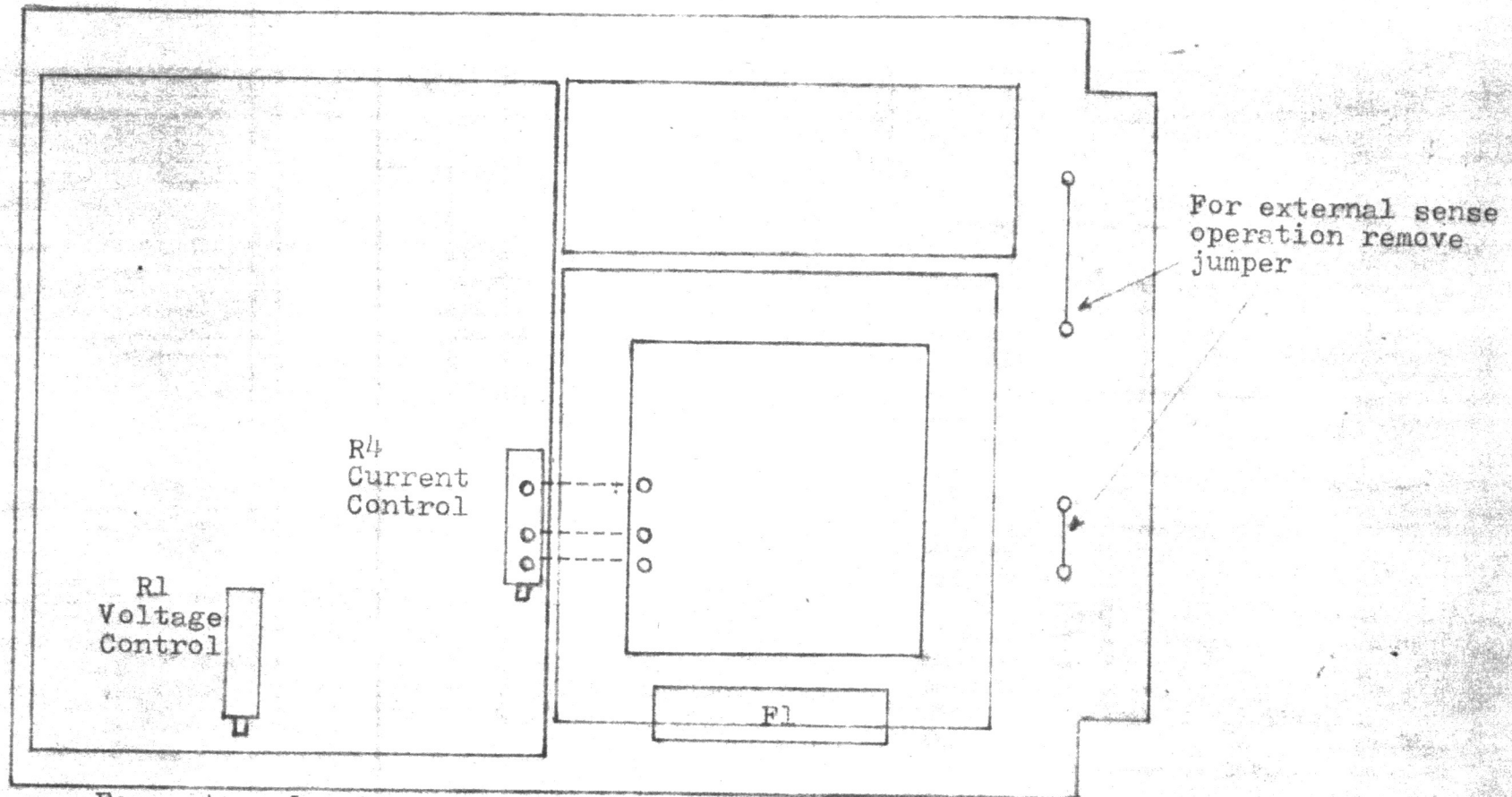
BOTTOM VIEW

MODEL	*R1
PC15-.1EM	15K
PC30-.5EM	30K
PC50-.2EM	50K
PC100-.1EM	100K
PC200-.05EM	200K
PC400-.02EM	400K

TITLE POWER SUPPLY		HOPE ELECTRONICS		
CONSTANT VOLTAGE		P.O. BOX 684		
CONSTANT CURRENT		285 CHANCEBRIDGE ROAD		
MODEL PC400-.02EM Dual Primary		PINE BROOK, N.J. 07058		
DRAWN	DATE 8-11-77	SIZE	DRAWING NUMBER	ISSUE
CHECKED	DATE		1737	
APPROVED	DATE			



# TOP VIEW



For external voltage and current control remove R1 & R4, install jumpers shown as dashed lines and connect control pots to contacts as shown on DWG. #1737

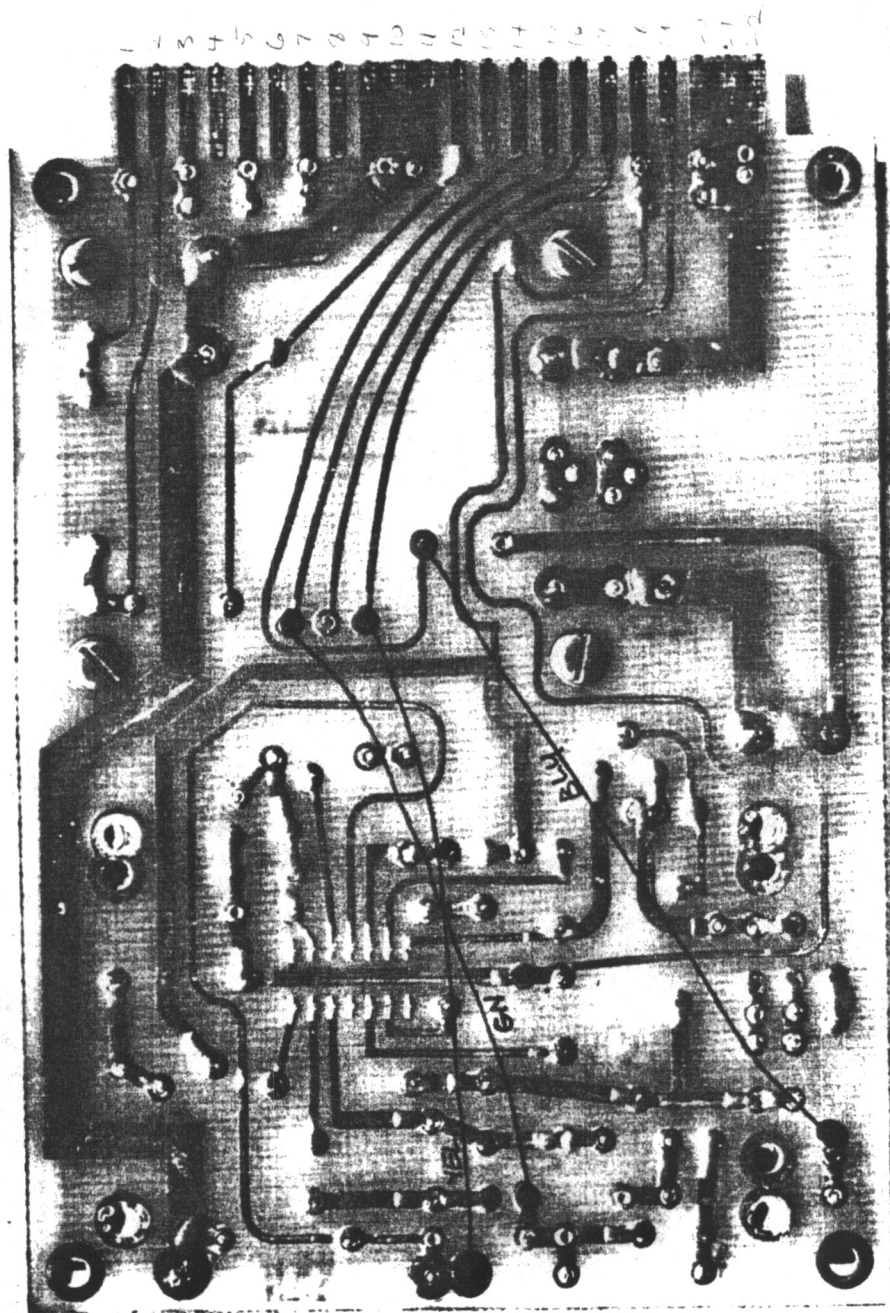
Note on 200 and 400V supplies DO NOT make measurements from + or - output to any points on Power Supply Card. Certain types of Meters can cause damage to supply.

TITLE POWER SUPPLY CONSTANT VOLTAGE CONSTANT CURRENT MODEL PC400-.02EM Dual Primary		HOPE ELECTRONICS P.O. BOX 684 285 CHANGEBRIDGE ROAD PINE BROOK, N.J. 07058		
DRAWN	DATE 8-11-77	SIZE	DRAWING NUMBER	ISSUE
CHECKED	DATE		1736	
APPROVED	DATE			









ADD JUMPERS

PC-400-02EM  
Modification  
Figure 2



COMP  
SIDE  
OF PC  
BOARD

RED

ADD DIODE  
+ RESISTOR

Remove  
wire  
+ transistor  
+ Heat Sink

YELLOW

GREEN

BLUE

PC400-102 FM  
Modification  
Figure 1



VCR SETUP

(REQUIRES VTB, VRG, VRM IN RESCAN CHASSIS & TEST CRT)

--SET VTB AS FOLLOWS:

ADDRESS	DATA
FF1000	<del>EO</del> C4 ✓
FF1004	1
FF1006	FFF
FF1020	1FF

--SET VRG AS FOLLOWS:

FF1400	7FF
FF1420	7FF
FF1440	7FF
FF1460	7FF
FF1480	7FF
FF14A0	7FF
FF14C0	0
FF14E0	7FF
FF1500	0
FF1520	7FF
FF1540	7FF
FF1560	7FF
FF1580	0
FF15A0	0

X

Y

--SET VRM AS FOLLOWS:

FF1800	0
FF1820	7FF
FF1840	7FF
FF1860	7FF
FF1880	7FF
FF18A0	0
FF18C0	7FF
FF18E0	7FF
FF1900	7FF
FF1920	7FF
FF1940	0
FF1960	7FF
FF1980	7FF
FF19A0	7FF
FF19C0	7FF
FF19E0	7FF

~~7FF~~ ✓

~~CHECK FOR BACKWARDS  
CLIP ZENER ROT OUT~~

--SET VCR AS FOLLOWS:

FF1C00	7FF
FF1C20	7FF
FF1C40	7FF
FF1C60	7FF
FF1C80	7FF
FF1CA0	7FF
FF1CC0	7FF



FF1CE0 7FF  
 FF1D00 7FF  
 FF1D20 7FF  
 FF1D40 7FF  
 FF1D60 7FF  
 FF1D80 0

VID: FF2000 0  
 FF2002 0  
 FF2004 0  
 FF2006 0  
 FF2008 0  
 FF200A 0  
 FF200C 0  
 FF200E 0  
 FF2010 0  
 FF2012 7FF  
 FF2018 4

(TZ = FF1960)  
 (V/Z = FF1920) ✓  
 (H/Z = FF1900)

ZERO DAC'S AS FOLLOWS (FOR ZERO VOLTS):

ADJUST	SCOPE	DAC#	
R6	TP-9	7	FF1CE0
R9	TP-10 *	9	FF1D20
R12	TP-11	11	FF1D60
R4	TP-12	10	FF1D40
R2	TP-13 *	8	FF1D00
R3	TP-14	6	FF1CC0
R7	TP-15	0	FF1C00
R10	TP-16	1	FF1C20
R13	TP-17	2	FF1C40
R15	TP-18	3	FF1C60
R16	TP-19	4	FF1C80
R17	TP-20	5	FF1CA0

Verify 0V at TP13 on VRG  
 (it can be reached without an extender on VRG)

VCR PERSPECTIVE DIVIDER SETUP:

- VCR ON EXTENDER
- NORMAL INITIALIZATION
- PUT FFF @ FF1920
- PUT SCOPE IN XY, X PROBE TO BOTTOM OF J5, Y TO BOTTOM OF J4.  
 GROUND INPUT AMPS ON SCOPE, PUT DOT IN LOWER RIGHT CORNER.
- UNGROUND INPUTS, SET TO 1V/CM, ADJ R20-D FOR LEFT SIDE OF TRACE TO BE APPROX. 0VDC.
- ADJUST R73 FOR CURVE TO CROSS A POINT 1.4 VOLTS UP AND 1.4 VOLTS OVER FROM ZERO. (EXPAND SENSITIVITY IF NECESSARY)
- RE-ADJUST R20-D FOR ZERO, AND R73 AS ABOVE.
- SET 7FF TO FF1920. VERIFY 7FF @ FF1960.
- ADJUST R3 ON VRM FOR TRACE TO SIT AT 1.4 V. UP AND 1.4 V. OVER FROM ZERO.

Turn R73 all the way CW then back 2 turns

AXIS DOT should be near this point.

TRIM DOT  
 If necessary



- SET 0 @ FF1960, RETURN SCOPE TO NORMAL.
- FINE TRIM R20-D FOR 0 VOLTS AT BOTTOM J4. IF Necessary.
- SCOPE TP-6.
- ADJUST R20-B FOR MINIMUM AC.
- ADJUST R20-C FOR ZERO DC OFFSET.
- SCOPE TP7, ADJUST R21-B, MINIMUM AC.
- ADJUST R21-C FOR ZERO DC OFFSET.

verify +5V at TP8

~~Ext Bus Multiplication Balances~~  
+ ~~Blanking Checks~~

### Ext Bus Multiplication Balances:

- load 35AD at FF1D80, scope TP3
- offset R59 B slightly to show zero point of ramp.
- adjust R59 A so zero point of ramp matches DC level when ramp is nulled with R59 B.
- Set R59 C for zero DC with 59 B nulled.
- Scope TP4, repeat as above, using R60 A-C
- Scope TP5, repeat as above, using R61 A-C

### Blanking Window Check:

Set the following:

FF1C00 - 0  
FF1CE0 - FFF  
FF1D00 - 0  
FF1D20 - FFF  
FF1D40 - 0  
FF1D60 - FFF  
FF1960 - ~~000~~ ~~000~~ 7FF  
FF1920 - 7FF

Scope TP6 and top of J6

(Top of J6 should be +5.)

Set FF1960 to ~~000~~ <sup>8C0</sup>. Blanking <sup>at J6</sup> should go low as

TP6 approaches either rail. adjusting FF1C00 and FF1CE0 should move the edges.

Scope TP7, observing same with FF FF1D00 and FF1D20

Return FF1960 to 7FF. Set FF1920 to FFF.



User 1104

VCR 101A, DC

+ Test CRT

## VCR Setup

P-1

(Requires VTB, VRG, VRM in Rescan classis)

- Set VTB as follows:

Address	Data
FF1000	EO
FF1004	1
FF1006	FFF
FF1020	1FF

- Set VRG as follows:

FF1400	7FF	
FF1420	"	
FF1440	"	
" 60	"	
" 80	"	
" A0	"	
FF14C0	0	X
FF14E0	7FF	
FF1500	0	Y
FF1520	7FF	
1540	7FF	
1560	7FF	

$$80 + A0 = 0$$

- Set VRM as follows -

FF1800	0
20	7FF
40	7FF
60	7FF







VIP: FF2000 0

2 0

4 0

6 0

8 0

A 6

C 0

E 6

10 0

12 7FF

14 4

TZ = FF1960

V/Z = FF1920

H/Z = FF1900

Vector EO8000



Zero DAC's as follows (for zero volts)

Adjust	Scope	DAC#	
R 6	TP-9	7	FFICE0
R 9	TP-10 *	9	FFID20
R 12	TP-11	11	FFID60
R 4	TP-12	10	FFID40
R 2	TP-13 *	8	FFID00
R 3	TP-14	6	FFIC60
R 7	TP-15	0	FFIC00
R 10	TP-16	1	FFIG20
R 13	TP-17	2	FFIC40
R 15	TP-18	3	FFIC60
R 16	TP-19	4	FFIC80
R 17	TP-20	5	FFICA0

- Center all Dip pots, connect XY scope set FF1920 (V to Z) to ~~FF~~ FFF scope bottom J5 (top trace) and J4 (bottom trace) turn FF1980 so top of V Ramp just approaches 0V.
- turn R73 max CCW
- adj R20-d for bottom trace = 0V. ok
- adj R20, 21-b for min signal on scope (mult bal)
- ~~adj R13 CW, zero R20-d, look for pattern:~~



~~put FFF at FF1920~~  
~~put A30 at FF1960~~

~~put Tek scope in XY @ 10V/cm~~  
~~Bottom  $55=X$ ,  $54=Y$ . Ground both~~  
~~scope inputs, set positions lower right,~~



~~Set scope inputs back to DC, adj R20-D for~~  
~~0V at left edge, adjust R73 to cause~~  
~~trace to hit 1.4-1.4. (adjust scope gain if~~  
~~unecessary) Return R20D and R73.~~

~~Connect scope probes to TP6+7. Ground scope~~  
~~inputs, center dot at center of graticule.~~  
~~adjust R20B and R21B for minimum waster~~  
~~adjust R20C and R21C for zero volts at zero waster.~~



## UCR perspective Divider Setup

- UCR on Extender
- Normal Initialization,
- Put FFF @ FF1920
- Put scope in XY, X probe to bottom of J5, Y to bottom J4. Ground input amps on scope, put dot in lower right corner.
- Unground inputs, set to 1v/cm, adj R20-D for left side of trace to be approx 0vdc
- Adjust R73 for curve to cross a point 1.4 ~~v~~ volts up and 1.4 volts over from zero. (expand sensitivity if necessary)
- Re-adjust R20-D for zero, and R73 as above
- Set 7FF to FF1920. Verify 7FF @ FF1960.
- Adjust R3 on URM for trace to sit at 1.4v up and 1.4v over from zero.
- Set 0 @ FF1960, Return scope to normal.
- Fine trim R20D for 0 volts at bottom J4,
- Adjust R20 B for minimum AC
- Adjust R20 C for zero DC offset,
- Scope TP7, Adjust R21 B, minimum AC
- Adjust R21 C for zero DC offset.

END

scope.  
TP-6 →



VAO Setup: user 1004  
VAO 100A.DC

- VAO on extender

~~-  $\overline{RST}$  to  $\overline{TRIP}$~~

Digital Oscillators:

FF2400 = 0 ~~0000~~, 02 = 10, 08 = 7FF,

0A = FFF, 0C = 7FF 0E = FFF

20 = 0, 22 = 0, 28 = 2

- Center ~~R21~~ CAG ~~D~~ ALL DIP POTS

- Scope TP3, verify sine wave, same at TP4.

- Set FF240E = 7FF, adj R75B for AC null TP3  
set R75C for Zero volts.

- Set FF240A = 7FF, adj R93-B for AC null, TP4  
set R93-C for Zero volts.

- Set 0A, 0E to FFF, set 20 + 22 to 8080.

- Set R75D for zero volts at bottom  
of full wave rectified sine wave at TP3

→ - Set R93-D for zero at TP4 as above.

Analog Oscillators:

FF2410 - ~~7FF~~, 12 - FFF, 14 - 7FF, 16 - FFF

18 - FFF, 1A - FFF, 24 - 0, 26 - 0, 2A - 101

- DUM pin 8 U35, set R8-D for 6.5 volts

- DUM pin 8 U31, set R8-A for 6.5 volts

Verify  $\approx 45\mu s$  sine wave at TP1 + 2

- Set FF2412 - 7FF, 16 - 7FF

- Scope TP1, set R39B for AC null, R39C, zero DC

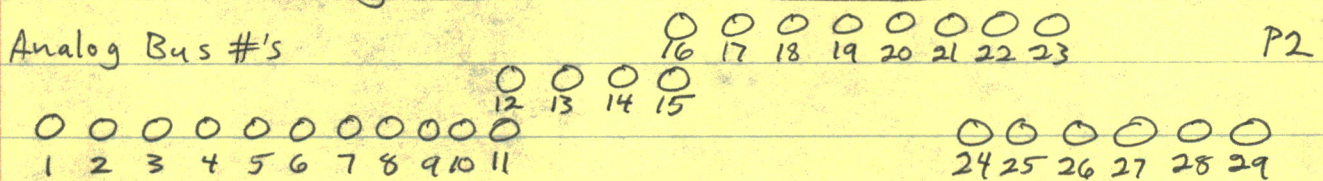
- Scope TP2, set R57B for AC null, R57C, zero DC



# VAO setup p2

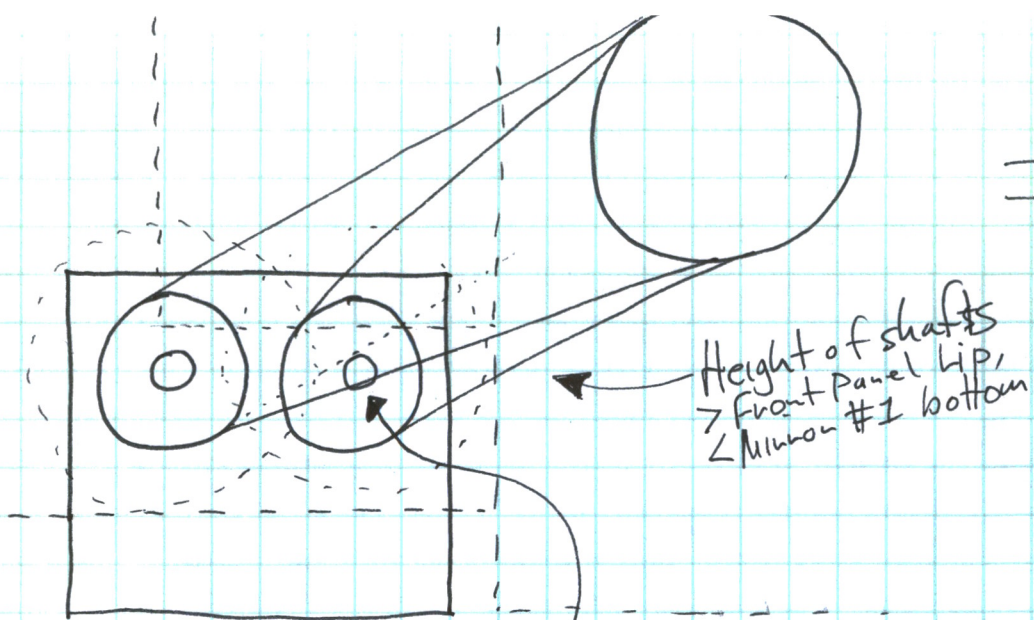
- FF2412 - FFF, 16 - FFF, 24 - 8080, 26 - 8080  
2A - 101, 18 - 0, 1A - 0.
- Set R39-D for bottom of FWR sine wave to zero volts at TP1
- Set R57-D for bottom of FWR sine wave to zero at TP2
- Set FF2428 to 1100, Adjust R8-B for 0 to +10 v Triangle at TP-1  
Adjust R1 for 0 to +10 v triangle at TP-2
- Set 28 to 2200 Adjust R1-C for 0 to +10 square at TP2, Adjust R8c for 0 to +10 " at TP1,

Connect osc 1-4 out to AB pads according to chart;

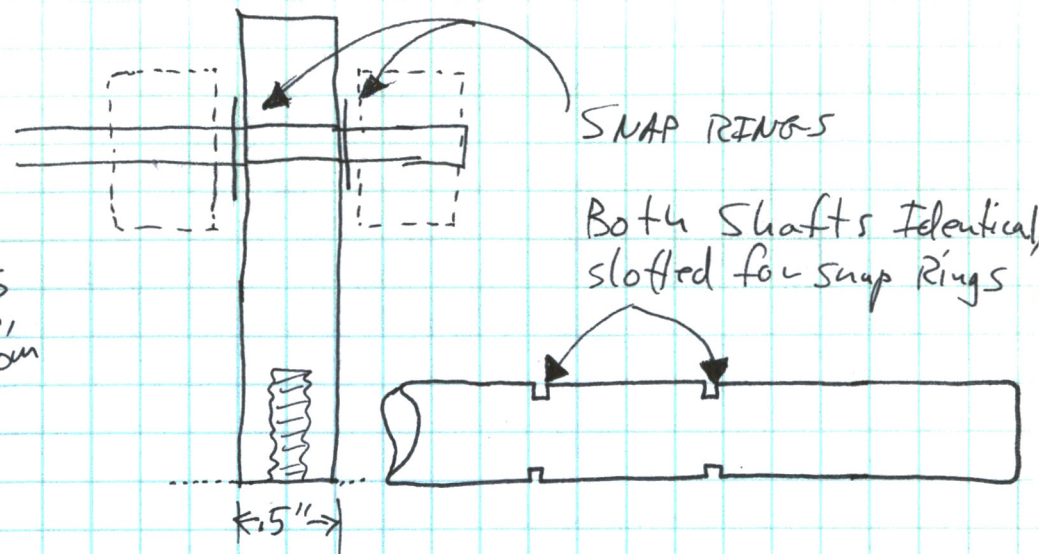
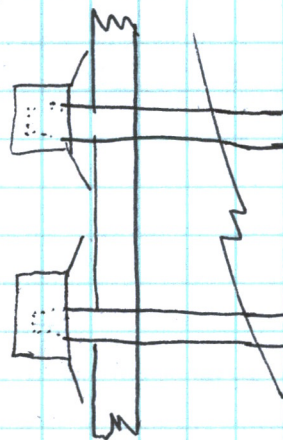


OSC	MASTER CHASSIS		RESCAN CHASSIS		
1A	#17	#21	#1	#5	#9
1B	#18	#22	#2	#6	#10
3	#19	#23	#3	#7	#11
4	#20	#24	#4	#8	#12
	BOARD 1	BOARD 2	BOARD 1	BOARD 2	BOARD 2

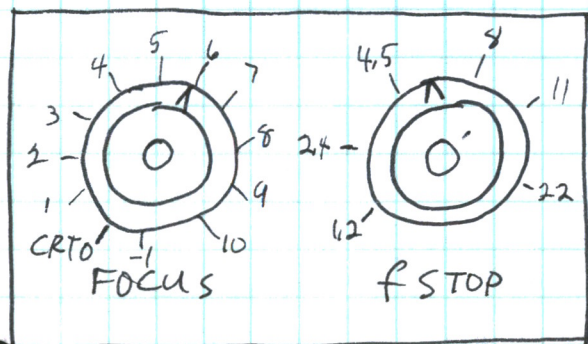




Angle to lens must  
 clear shaft here.  
 Adjust spacing  
 to accomodate



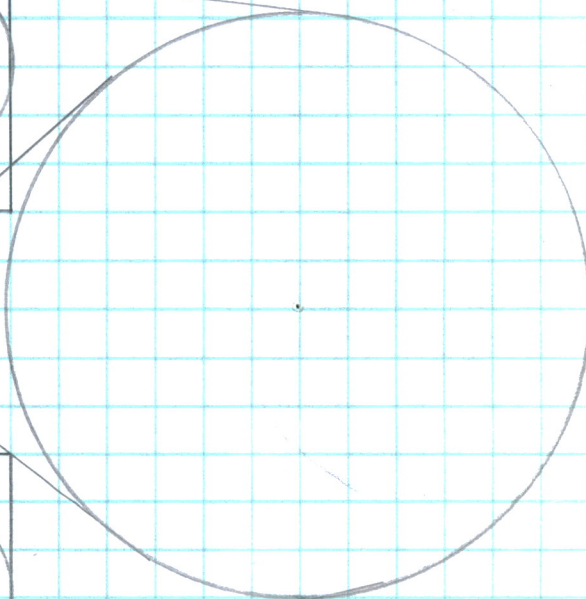
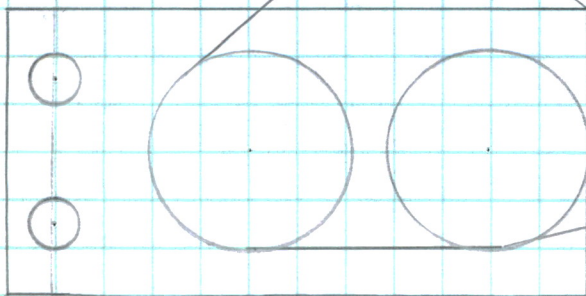
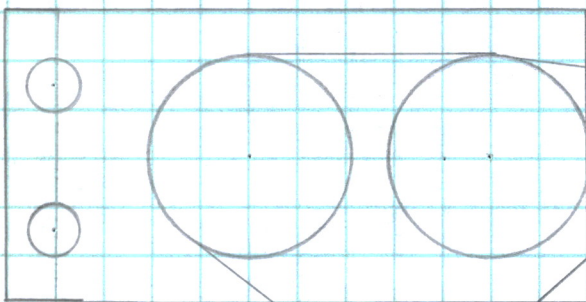
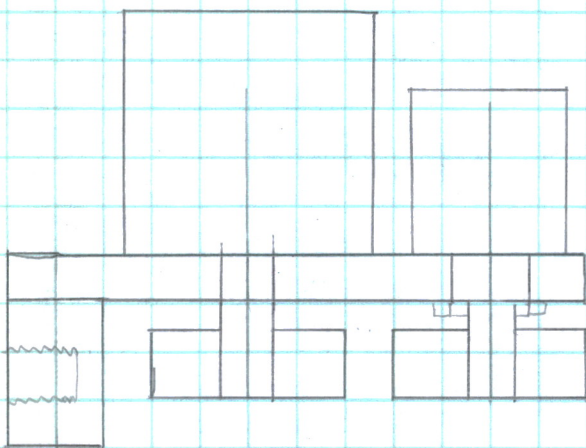
Max Size of Pulley  
 = Size of Lens Pulley



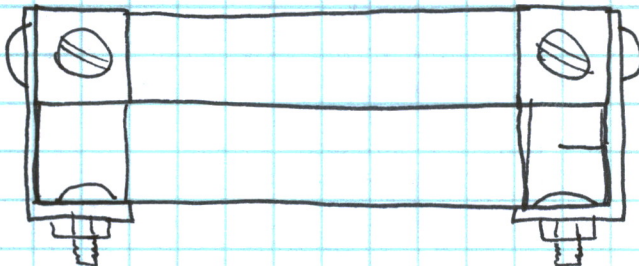
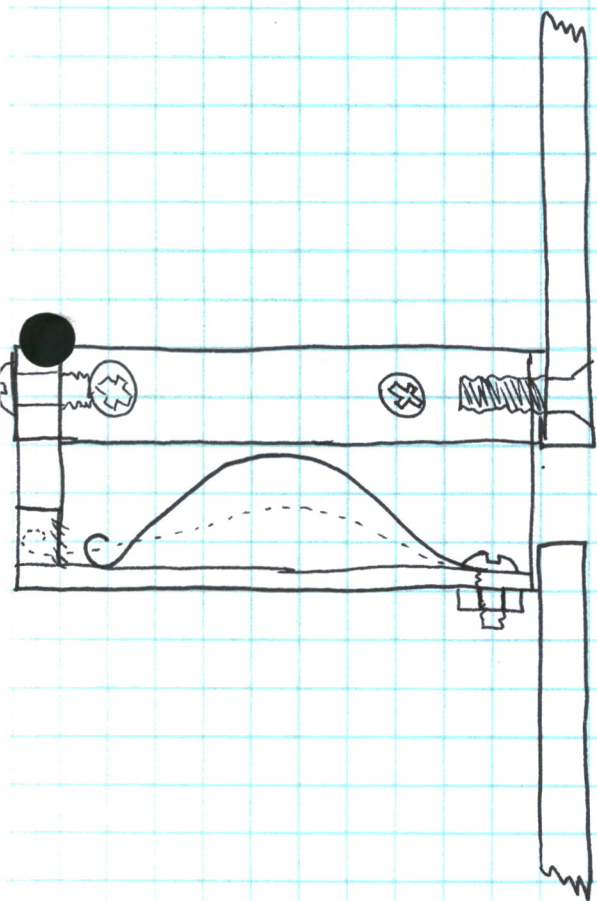
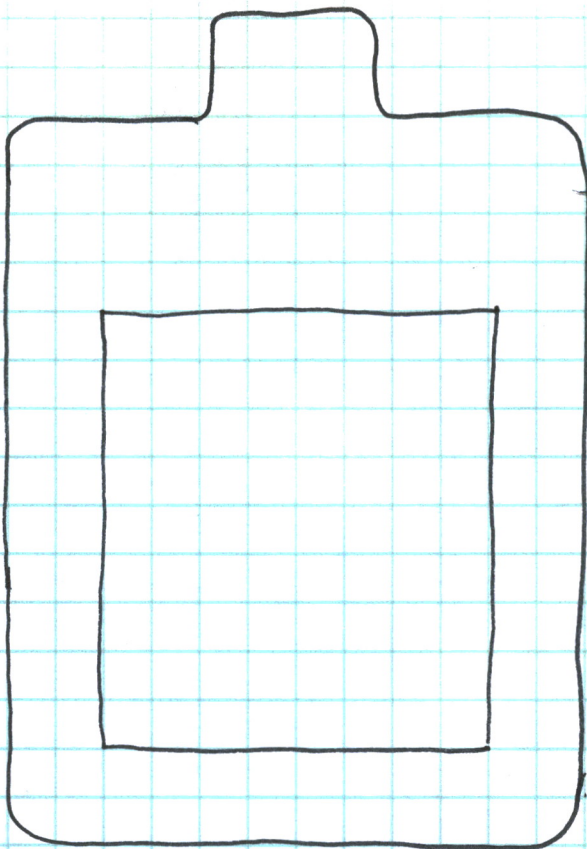
Camera Focus + f stop  
 Remote Controls

done 11/15/82



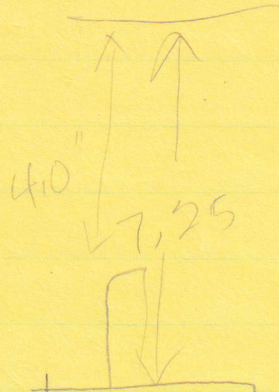




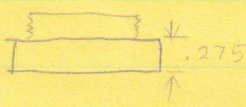
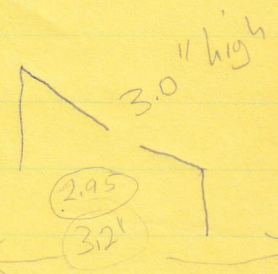




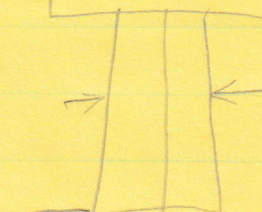
$\frac{1.25}{6.25}$   
 $\frac{1.875}{6.25}$



7.5"  
 7.25



1.82



4.775  
 4.525

7.375"

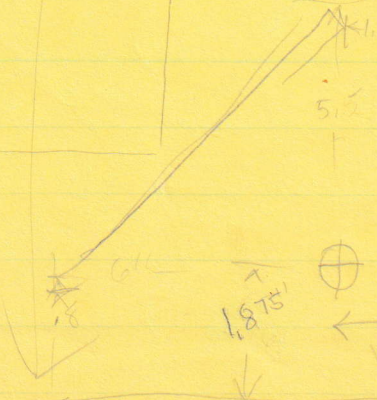
1.60

2.70

2.50  
 2.30

3.565

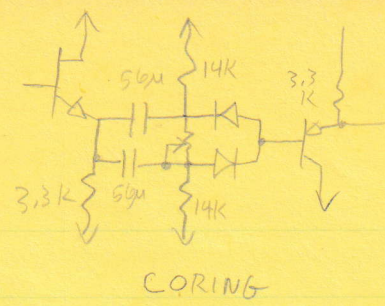
2.025"



0.95  
 1.20  
 2.98  
 2.05



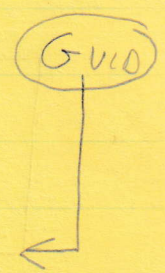
CI 2H Delay  
 CORNING  
 42135-0286



714-771-0260

Cam Cable

- J2 Video (blk + wh bal, masking)
- J4 Interface (gamma, blk + wh clip)
- J5 Sync + Enc
- J3 Enhancer (GN PROC + DLY)



~~5160~~  
~~408 732 5050~~

av  
 Raleigh NC. - Killough  
 919-876-1100

015

VERIFIED  
 1



Name	Desig.	Schematic	PC Design	Boards	Parts	Static Test	Software module	Dynamic Test	PAL Check
Timing + Blanking	VTB	Done	Done	4 <sup>*</sup> (4)	90%	by 7/19	by 7/26	by 9/27	by 7/19
Raster Generator	VRG	Done	Done	4 <sup>*</sup> (3)	10%	by 9/20	by 7/26	by 11/1	by 9/20
Rotation matrix	VRM	Done	by 8/9	by 8/9	by 8/9	by 11/11	by 9/6	by 11/1	by 11/11
CRT Driver	VCR	Done	by 8/30	by 8/30	by 8/30	by 11/8	by 9/6	by 12/6	by 11/8
operator display generator	VDG	Done	Done	4 <sup>*</sup> (4)	90%	by 7/12	by 10/11	by 10/11	by 10/11
Vector generator	VUG	Done	Done	by 7/19	by 7/19	by 9/27	by 12/27	by 12/27	by 9/27
VIDEO Board	VID	by 8/30	by 11/1	by 11/1	by 11/1	by 12/20	by 12/6	by 12/27	by 12/20
Communication Interface	UCI	done	done	4 (4)	95%	done	by 9/6	by 11/1	<del>by 11/1</del>
Console connection	VCC	done	by 8/9	by 8/9	by 8/9	by 11/25	by 11/29	by 11/29	—
Animation Oscillator	VAO	by 8/30	by 11/1	by 11/1	by 11/1	by 12/20	by 11/1	by 12/27	—



TABLE 2. J2/P2 Pin Assignments for

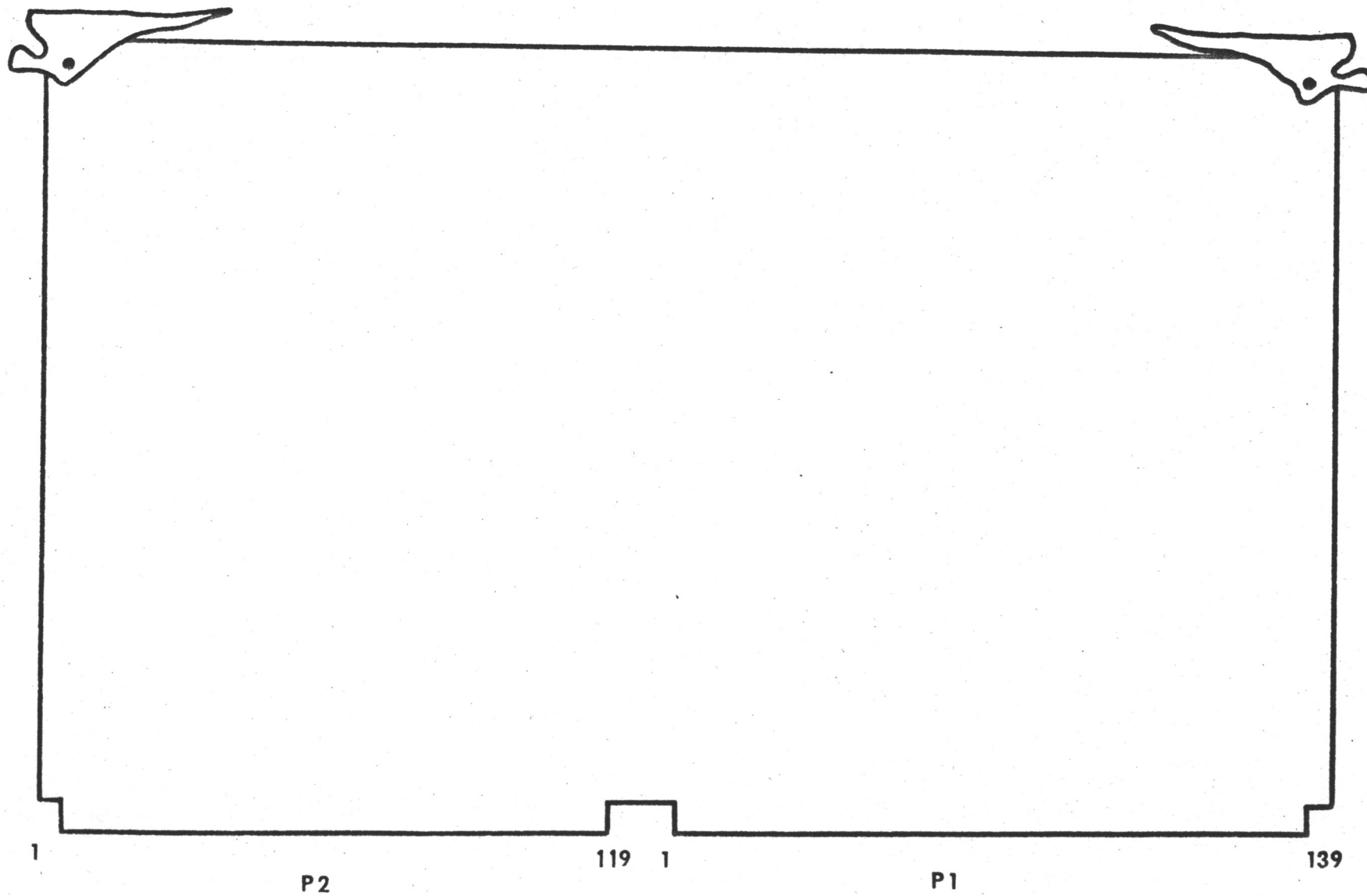
(cont'd)

ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
97		98	
99		100	
101		102	
103		104	
105		106	
107		108	
109		110	
111		112	
113		114	
115		116	
117		118	
119		120	
NOTE: Pins 17 through 66 together by the backplane. are not bussed			



BOARD \_\_\_\_\_

VER. \_\_\_\_\_





VERSEFX J2/P2 PIN ASSIGNMENTS (MODIFIED VERSABUS)

COMPONENT SIDE		SOLDER SIDE	
PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	+5V	8	+5V
9	+5V	10	+5V
11	+12V	12	+12V
13	GND	14	GND
15	-12V	16	-12V
17	AB1	18	
19	AB2	20	
21	AB3	22	
23	AB4	24	
25	AB5	26	
27	AB6	28	
29	AB7	30	
31	AB8	32	
33	AB9	34	
35	AB10	36	
37	AB11	38	AB17
39	AB12	40	AB18
41	AB13	42	AB19
43	AB14	44	AB20
45	AB15	46	AB21
47	AB16	48	AB22
49		50	AB23
51		52	AB24
53		54	AB25
55		56	AB26
57		58	AB27
59		60	AB28
61		62	AB29
63		64	AB30
65		66	AB31
67	-15V	68	-15V
69	+15V	70	+15V

NOTE: Pins 17 through 66 are not bussed across by the backplane.  
ALL other pins are.

AB1 - AB31 ANALOG BUS LINES



(Page 2) VERSEFX J2/P2 PIN ASSIGNMENTS (MODIFIED VERSABUS)

COMPONENT SIDE		SOLDER SIDE	
PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
71		72	
73	RB*	74	
75	VI*	76	VR*
77	HR*	78	ZR*
79	HI*	80	VALE*
81	HC*	82	LHC*
83	BKG*	84	S1*
85	S2*	86	S3*
87	S4*	88	LB*
89	SB*	90	FI*
91	VAL*	92	PRHR*
93	HB	94	GHR*
95		96	
97	GND	98	GND
99		100	
101		102	
103		104	
105		106	
107		108	
109		110	
111		112	
113		114	
115		116	
117		118	
119		120	

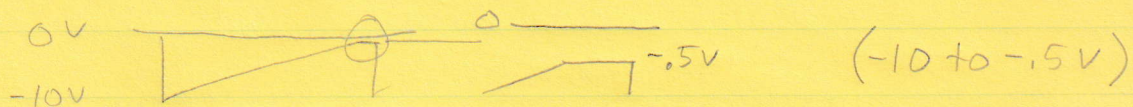
\* Denotes active LOW

RB = RASTER RELATIVE BLANKING  
 VI = VERTICAL INTERVAL  
 VR = VERTICAL RESET  
 HR = HORIZONTAL RESET  
 ZR = Z RESET  
 HI = HI-RESOLUTION SYNC MODE  
 VALE= VERTICAL AXIS LOCATE ENABLE  
 HC = HORIZONTAL CLAMP  
 LHC= LO-RESOLUTION HORIZONTAL CLAMP  
 BKG= BLANKING TO CRT  
 S1-S4 = SECTION ADDRESS LINES  
 LB = LO-RESOLUTION BLANKING  
 SB = SCREEN RELATIVE BLANKING  
 FI = FIELD IDENTIFICATION  
 VAL= VERTICAL AXIS LOCATE  
 PRHR= PROGRAMMABLE HI-RESOLUTION HORIZONTAL RESET  
 GHR= GRAPHICS HORIZONTAL RESET  
 HB = HORIZONTAL BLANKING

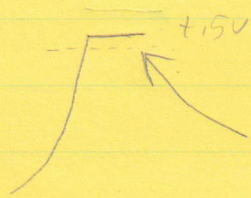
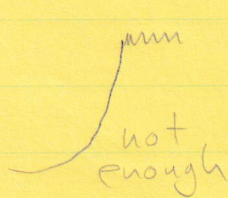


## Perspective Divider notes:

Put Z into CRT Board so that you get V Ramp like this:



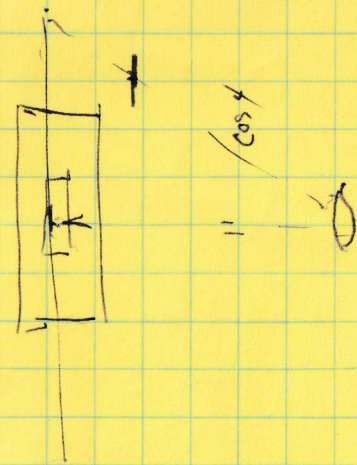
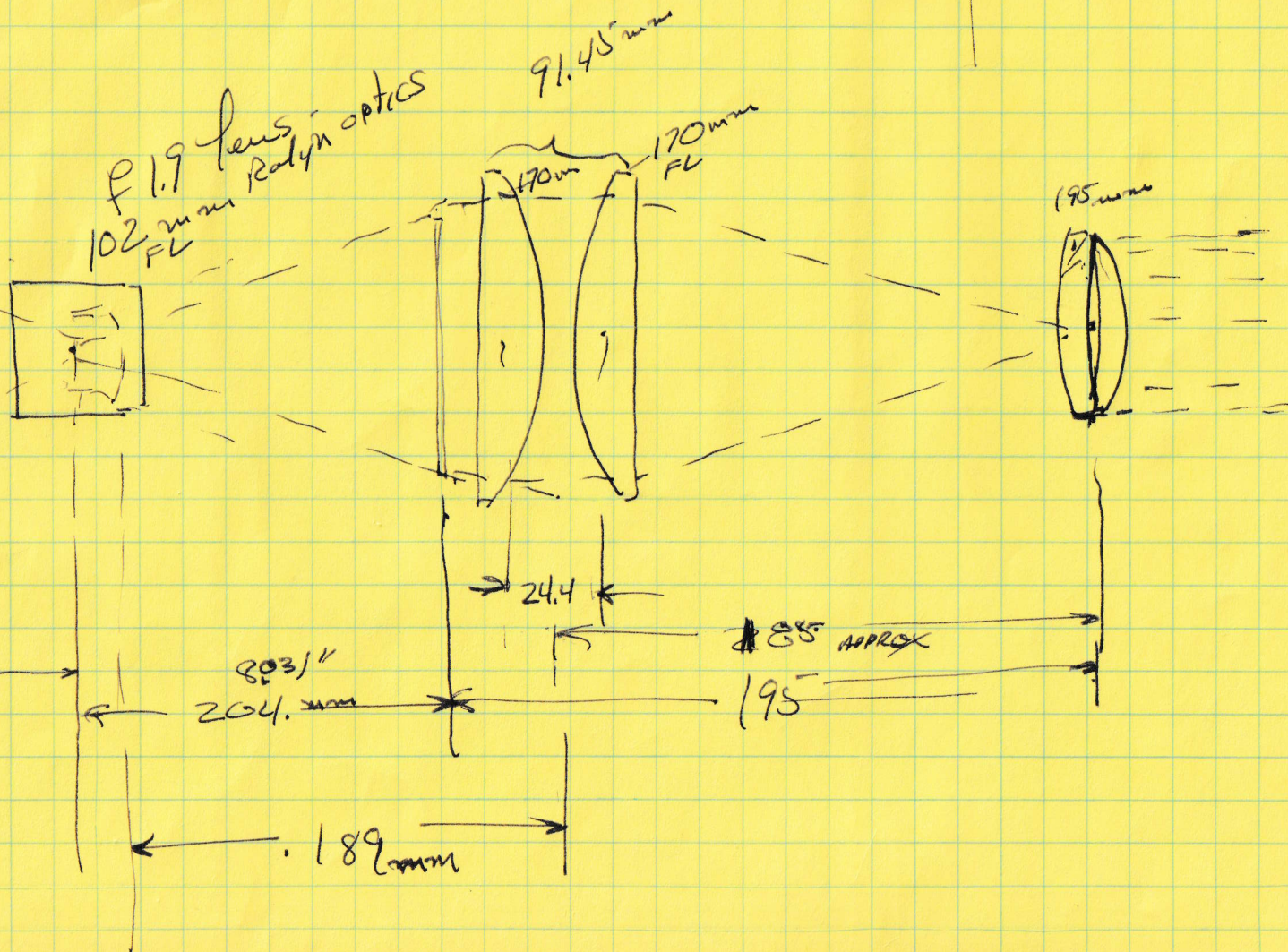
Scope TP-2,  
Adjust R73 so that noise  
just gets clipped:



Set R20 so that  
clipped shelf is  
at +.5V



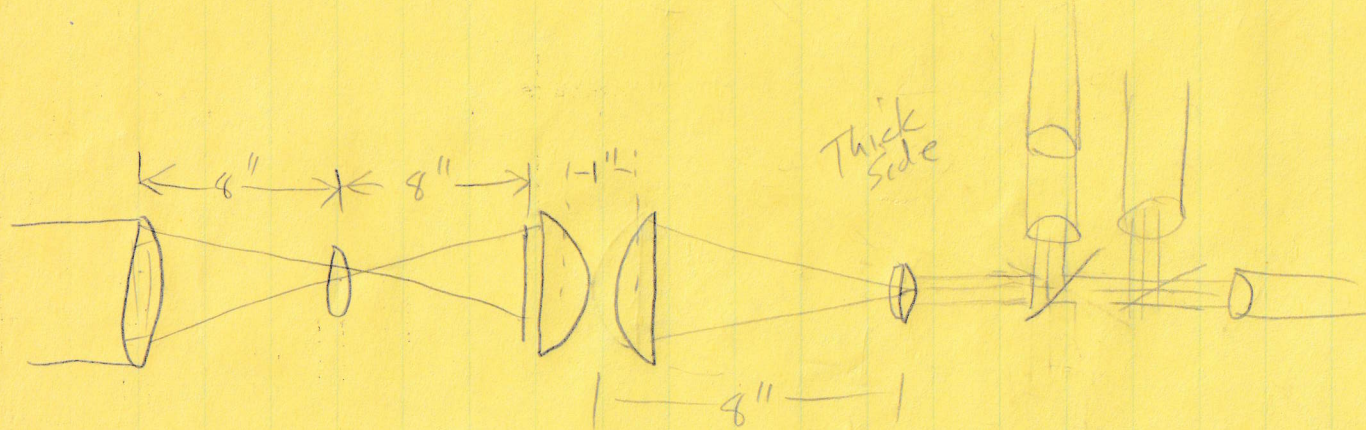
SCOPE





41  
3  
164

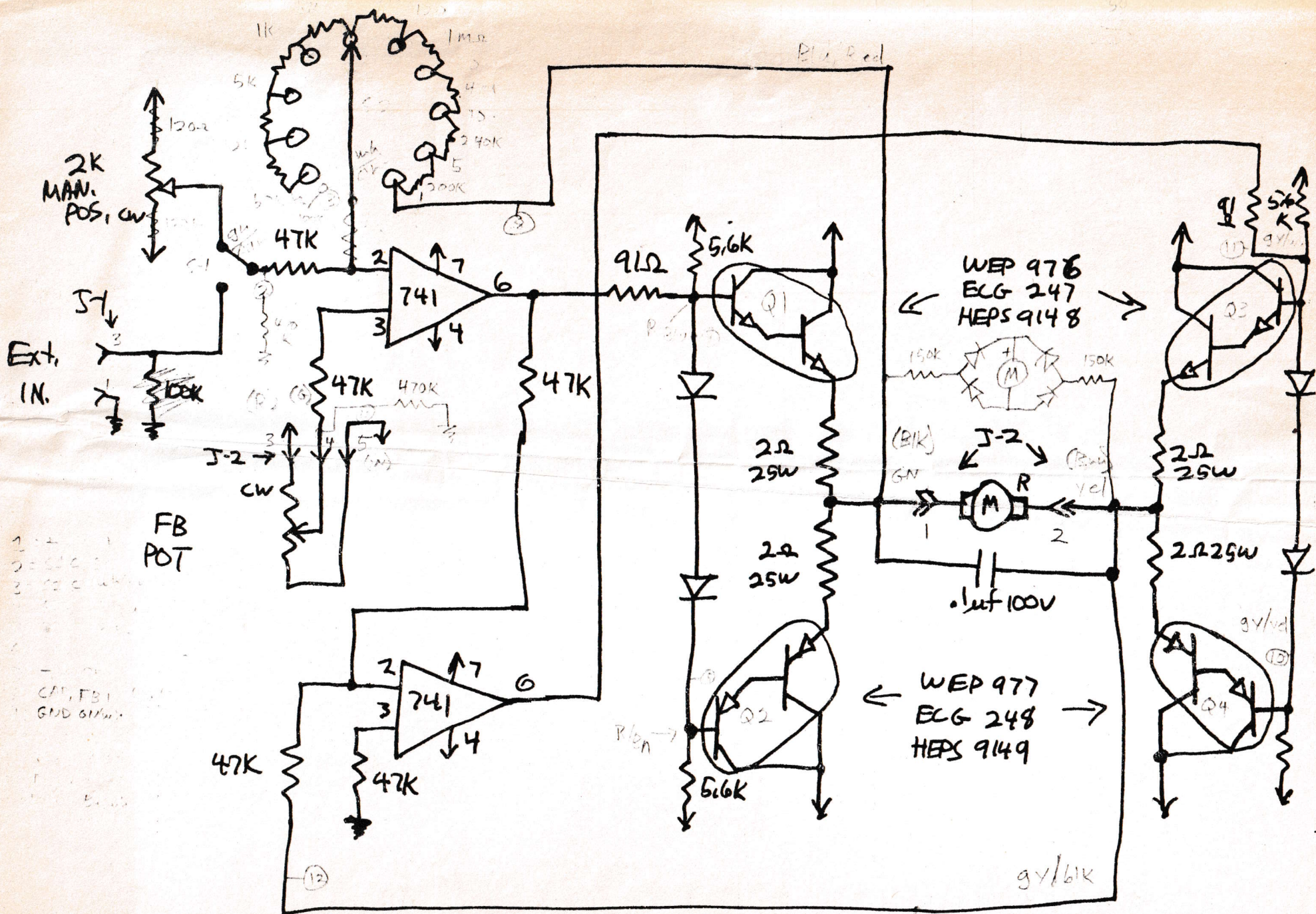
102 mm f1.9 Polyn 8" from CRT  
.031



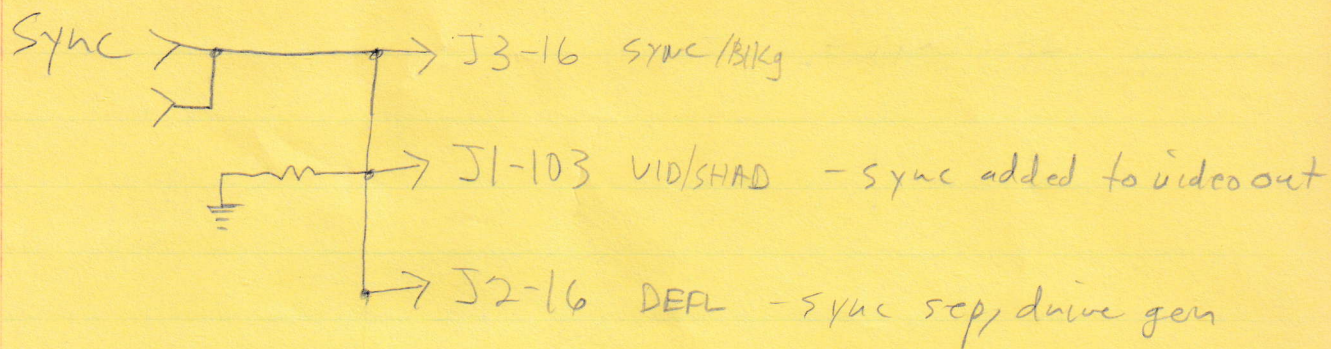








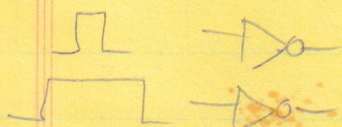




HT u1 in

VT TP7

CB + C4





In references for part: RV 10K BOURNS 3006, overlapping references: R14, over part: RV 5K BOURNS 3006  
In references for part: RV 10K BOURNS 3006, overlapping references: R15, over part: RV 5K BOURNS 3006  
In references for part: C .1UF 50V, overlapping references: C68, over part: C .1UF 50V  
In references for part: C 18PF 200V, overlapping references: C81, over part: C .1UF 50V

VIB -  
File errors



In references for part: RV 10K BOURNS 3299, overlapping references: R83-84, over part: R 10K OHM 1/4W 2%

VRG -  
File errors



This file contains the fixes for VCI100A. All changes in this file should be made on version 'A' of the board.

1) Problem: The signals VB\_DS0 and VB\_DS1 need to be reversed everywhere except at UG5-7.

Fix: Cut wire from UG5-7 on solder side.  
Cut wire from UA7-5 on solder side.  
Solder Jumper from UA7-5 to UC4-13.  
Solder Jumper from UA7-7 to UC4-11.

2) Problem: The signals DMA\_A00 and DMA\_A00\* need to be reversed.

Fix: Cut wire on LEFT side of UB15-11 on solder side.  
Cut wire from UB15-10 on solder side.  
Solder Jumper from UB15-11 to UC15-11.  
Solder Jumper from UB15-10 to UC15-13.

3) Problem: No pullups on the RAM decoders address inputs.

Fix: Solder Jumper from RFG1-9 to JB6-4.  
Solder Jumper from RFG1-10 to JB6-3.

4) Problem: UC22-2 and UC24-1 should be DMA\_GRNTD\_LB instead of DMA\_GRNTD\_VB.

Fix: Cut wire on RIGHT side of UC24-1 on solder side.  
Cut wire BELOW UC22-2 on solder side.  
Solder Jumper from UC29-2 to UG13-3.  
Solder Jumper from UC31-1 to UC22-1.  
Solder Jumper from UC31-13 to UC24-1.

5) Problem: Include DMA VERSAbus access rights as bit 3 of the DMA mode register.

Fix: Solder Jumper from UB14-14 to JB8-2.

6) Problem: Reset push-button switch holes and connections were layed out wrong.

Fix: Wire push button switch descretely:

	0	0	Mounting Holes
(1)	(2)	(3)	
0	0	0	
(NC)	(COM)	(NO)	

Hole 1 should be connected to the Normally Connected switch contact.  
Hole 2 should be connected to the Common switch contact.  
Hole 3 should be connected to the Normally Open switch contact.

7) Problem: Read I/O DTACK and write I/O DTACK were reversed.

Fix: Cut wire from UC7-5 on solder side.  
Cut wire from UA7-10 on solder side.  
Solder Jumper from UC12-11 to UC7-10.  
Solder Jumper from UC11-9 to UC7-5.

8) Problem: Tranceivers that interface the TMS9914A to the local data bus didn't have the output enables decoded.



Fix: Cut wire from UD4-19 on solder side.  
Cut wire from UD5-19 on component side.  
Solder Jumper from UD7-6 to UD4-19.  
Solder Jumper from UD7-8 to UD5-19.  
Solder Jumper from UD7-4 to UD7-9.  
Solder Jumper from UA19-8 to UD7-9.  
Solder Jumper from UC15-7 to UD7-5.  
Solder Jumper from UC15-9 to UD7-10.  
Solder Jumper from UG11-10 to UA19-10.  
Solder Jumper from UC1-4 to UA19-9.

9) Problem: RS2 and RS0 reversed on TMS9914A chip.

Fix: Cut wire from UD1-6 on component side.  
Cut wire from UD1-8 on component side.  
Solder Jumper from UD1-6 to UA6-16.  
Solder Jumper from UD1-8 to UA6-12.

10) Problem: REN and IFC tied together on TMS9914A and 75162A.

Fix: Cut wire between UD1-22 and UD1-23 on solder side.  
Cut wire between UD1-23 and UD3-20 on solder side.  
Cut wire between UD3-20 and UD3-19 on solder side.  
Solder Jumper from UD1-22 to UD3-20.  
Solder Jumper from UD1-23 to UD3-19.

11) Problem: Enable input on 9519A is positive logic and it was tied to ground.

Fix: Cut wire between UG7-14 and UG7-13 on solder side.

12) Problem: Interrupt acknowledge's level decoder wired incorrectly to interrupt response's Jumper block.

Fix: Cut wire from UG3-15 on solder side.  
Solder Jumper from UG3-7 to JB4-7.

13) Problem: When Multi-Wire reversed the power and ground on the AM2940 chips, they forgot to change the wired ground connections to the pins on the chips, thus pins that should have been grounded were tied to VCC.

Fix: Cut wire from UB3-8 on solder side.  
Cut wire from UB4-8 on solder side.  
Cut two wires from UB4-8 on solder side.  
Solder Jumper from UB3-22 to UB3-20.  
Solder Jumper from UB4-22 to UB4-20.  
Solder Jumper from UB5-22 to UB5-20.  
Solder Jumper from UB5-20 to UB5-9.

14) Problem: Multi-wire mis-wired IO\_WRX to the front panel logic.

Fix: Cut wire on BOTH sides of UF4-13 on solder side.  
Solder Jumper from UB16-11 to UF4-9.  
Solder Jumper from UC12-10 to UF4-13.

15) Problem: There is an undocumented GLITCH on the 'GINT' line of the AMD 9519A. This caused a second interrupt request to follow the end of the first request. The fix was to insure the requests are at least 200ns long.

Fix: Cut wire on BOTH sides of UG10-2 on solder side.  
Cut wire from UG10-1 on solder side.  
Cut wire from UG10-3 on solder side.  
Cut wire from UG10-5 on solder side.



Solder Jumper from UG10-1 to UG10-13.  
Solder Jumper from UG10-3 to UG10-11.  
Solder Jumper from UG10-5 to UG10-12.  
Solder Jumper from UG10-10 to UG10-14.  
Solder Jumper from UG10-9 to UG5-3.  
Solder Jumper from UG11-4 to UG10-2.  
Solder Jumper from UG11-4 to UA19-13.  
Solder Jumper from UG10-1 to UA19-11.  
Solder Jumper from UG5-12 to UA19-12.

16) Problem: BGXOUT should be a TTL T.P. output and a 74S38 was used on the line. It needs to have a pullup.

Fix: Solder Jumper from UG2-8 to RPG1-8.

17) Problem: UC32 had pins 8 and 10 reversed.

Fix: Cut wire on BOTH sides of UC32-8 on solder side.  
Cut wire from UC32-10 on solder side.  
Solder Jumper from UC25-3 to UC32-8.  
Solder Jumper from UC20-5 to UC32-10.  
Solder Jumper from UC6-2 to UC32-10.



Total	Part Name	Distributor	Manufacturer	Part Number	P. O. Number	Quantity	Price	Due Date
6	25LS2521	HAMILTON	AMD	25LS2521				
9	25S08	HAMILTON	AMD	25S08				
2	2/16	HAMILTON	ANY	2/16				
1	30MHZ OSC	SHELLEY HAMILTON	DALE DALE	XO-13B30 XO-13B30				
1	74128	HAMILTON	ANY	74128				
1	74148	HAMILTON	ANY	74148				
1	7433	HAMILTON	ANY	7433				
2	74F521	HAMILTON	FAIRCHILD	74F521				
3	74LS00	HAMILTON	ANY	74LS00				
2	74LS02	HAMILTON	ANY	74LS02				
2	74LS04	HAMILTON	ANY	74LS04				
1	74LS08	HAMILTON	ANY	74LS08				
2	74LS10	HAMILTON	ANY	74LS10				
1	74LS11	HAMILTON	ANY	74LS11				
1	74LS112	HAMILTON	ANY	74LS112				
1	74LS157	HAMILTON	ANY	74LS157				
1	74LS158	HAMILTON	ANY	74LS158				
6	74LS161	HAMILTON	ANY	74LS161				
2	74LS20	HAMILTON	ANY	74LS20				
5	74LS240	HAMILTON	ANY	74LS240				
5	74LS244	HAMILTON	ANY	74LS244				
2	74LS245	HAMILTON	ANY	74LS245				
3	74LS32	HAMILTON	ANY	74LS32				
4	74LS373	HAMILTON	ANY	74LS373				
4	74LS74A	HAMILTON	ANY	74LS74A				
1	74LS85	HAMILTON	ANY	74LS85				



Total	Part Name	Distributor	Manufacturer	Part Number	P. O. Number	Quantity	Price	Due Date
8	74LS86	HAMILTON	ANY	74LS86				
3	74S02	HAMILTON	ANY	74S02				
3	74S112	HAMILTON	ANY	74S112				
1	74S139	HAMILTON	ANY	74S139				
2	74S153	HAMILTON	ANY	74S153				
5	74S161	HAMILTON	ANY	74S161				
1	74S188	HAMILTON	ANY	74S188				
4	74S189	HAMILTON	ANY	74S189				
1	74S195	HAMILTON	ANY	74S195				
2	74S240	HAMILTON	ANY	74S240				
8	74S299	HAMILTON	ANY	74S299				
1	74S32	HAMILTON	ANY	74S32				
2	74S37	HAMILTON	ANY	74S37				
1	74S38	HAMILTON	ANY	74S38				
8	Am27S191C	HAMILTON	AMD	Am27S191C				
134	C .10F 50V CER .25S	HAMILTON	KEMET	C321C104M5R5CA				
1	DP8408	HAMILTON	NATIONAL	DP8408				
1	JB-14							
1	JB-2							
1	JB-4							
1	MC68B09	HAMILTON	MOTOROLA	MC68B09				
3	MC68B21	HAMILTON	MOTOROLA	MC68B21				
8	MCM6665A-15	HAMILTON	MOTOROLA	MCM6665A-15				
5	R 1K OHM 5% 1/8W							
1	R 1K OHM SIP-6	HAMILTON	BOURNS	4306R-101-102				
2	R 2K OHM 5% 1/8W	HAMILTON	ANY	?				
5	R 3.3K OHM SIP-10	HAMILTON	BOURNS	4310R-101-332				



Total	Part Name	Distributor	Manufacturer	Part Number	P. O. Number	Quantity	Price	Due Date
38	SOCKET-14 ST	HAMILTON	AUGUT	214-AG-49D				
45	SOCKET-16 ST	HAMILTON	AUGUT	216-AG-49D				
41	SOCKET-20 ST	HAMILTON	AUGUT	220-AG-49D				
25	SOCKET-24 ST	HAMILTON	AUGUT	224-AG-49D				
2	SOCKET-28 ST	HAMILTON	AUGUT	228-AG-49D				
6	SOCKET-40 ST	HAMILTON	AUGUT	240-AG-49D				
1	SOCKET-48 ST	HAMILTON	AUGUT	224-AG-49D (QTY X2)				
1	SW DIP-6							
1	SW DIP-8							
1	SW DPS1 PB							
17	TMM2016	JACO	TOSHIBA	TMM2016				
2	UPD7220	ANTHEM	NEC	UPD7220				



# VDG

## Component List for VDG100

Page 1

Reference No's	Total	Part Name	Part Type	Description
CA1-15, CB1-20, CC1-15, CD1-22, CE1-23, CF1-17, CG1-22	134	C .1UF 50V CER .256	CAPACITOR	.1 UF 50V CERAMIC CAPACITOR
JB1	1	JB-14	JUMPER BLK	14 PIN JUMPER BLK
JB2	1	JB-2	JUMPER BLK	2 PIN JUMPER BLK
JB3	1	JB-4	JUMPER BLK	4 PIN JUMPER BLOCK
PB1	1	SW DPST PB	SWITCH	DPST PUSH-BUTTON SWITCH
RC2-3	2	R 2K OHM 5% 1/8W	RESISTOR	2K OHM 5% 1/8W RESISTOR
RD1, RE1, RF1-2, 11	5	R 1K OHM 5% 1/8W		No description found in cross ref file
RPA1-3, RPC1-2	5	R 3.3K OHM SIP-10	RES NET	3.3K OHM 10 PIN RESISTOR NETWORK
RPG1	1	R 1K OHM SIP-6	RES NET	1K OHM 6 PIN RESISTOR NETWORK
SUA1, 20-22, SUD1, SUE1	6	SOCKET-40 ST	SOCKET	40 PIN SOLDER TAIL SOCKET
SUA2-7, SUB8-10, 12-14, SUC1-10, SUD2-3, 16-17, 22, SUE2-3, 15-16, 21, SUF1-2, 5-6, SUG13-14, 18, 24-25	41	SOCKET-20 ST	SOCKET	20 PIN SOLDER TAIL SOCKET
SUA8, SUB2, 16-23, SUC13-15, 17-18, SUD5, SUE26, SUF3-4, 7-14, 17, SUG2-6, 8-9, 11-12, 15-17, 19-22, 26	45	SOCKET-16 ST	SOCKET	16 PIN SOLDER TAIL SOCKET
SUA9-17, SUB3-7, 11, 24, SUC11-12, 16, SUD4, 6-7, 23-26, SUE4-6, 22-25, SUF15-16, SUG7, 10, 23	38	SOCKET-14 ST	SOCKET	14 PIN SOLDER TAIL SOCKET
SUA18-19	2	SOCKET-28 ST	SOCKET	28 PIN SOLDER TAIL SOCKET
SUB1, SUD8-15, 18-21, SUE7-14, 17-20	25	SOCKET-24 ST	SOCKET	24 PIN SOLDER TAIL SOCKET
SUB15	1	SOCKET-48 ST	SOCKET	48 PIN SOLDER TAIL SOCKET (2-24 PIN SOCK
SW1	1	SW DIP-8	SWITCH	8 POSITION DIP SWITCH
SW2	1	SW DIP-6	SWITCH	6 POSITION DIP SWITCH



## Component List for VDG100

Page 2

Reference No's	Total	Part Name	Part Type	Description
UA1	1	MC68E09	IC	2 MHZ 6809 MICRO-PROCESSOR
UA2, UB14	2	74LS245	IC	OCTAL BUS TRANSCEIVER
UA3-5, UB12-13	5	74LS244	IC	OCTAL BUS DRIVER
UA6-7, UC8-10, UG18	6	25LS2521	IC	8 BIT COMPARATOR
UA8	1	74S188	IC	32X8 PROM
UA9, UB5	2	74LS20	IC	DUAL 4-INPUT NAND GATE
UA10, UB4	2	74LS10	IC	TRIPLE 3-INPUT NAND GATE
UA11, 13, UB24	3	74LS32	IC	QUAD 2-INPUT OR GATE
UA12, UB7	2	74LS04	IC	HEX INVERTER
UA14-15, UE25	3	74LS00	IC	QUAD 2-INPUT NAND GATE
UA16, UB11, UG10	3	74S02	IC	QUAD 2-INPUT NOR GATE
UA17	1	74LS08	IC	QUAD 2-INPUT AND GATE
UA18-19	2	2716	IC	2KX8 EPROM
UA20-22	3	MC68B21	IC	2 MHZ PIA
UB1, UB8-15, UE7-14	17	TMM2016	IC	2KX8 STATIC RAM
UB2	1	74LS158	IC	QUAD 2-1 INV DATA MULTIPLEXERS
UB3	1	74S38	IC	QUAD 2-INPUT NAND BUFFER W/OC OUTPUT
UB6	1	74LS11	IC	TRIPLE 3-INPUT AND GATE
UB9-10, UF1-2, 5-6, UG24-25	8	74S299	IC	8 BIT SHIFT REGISTER
UB15	1	DP8408	IC	DYNAMIC RAM REFRESH CONTROLLER
UB16-23	8	MCM6665A-15	IC	150 ns 64K DYNAMIC RAM
UC1, 3, 5-7	5	74LS240	IC	OCTAL BUS DRIVER
UC2, 4	2	74S240	IC	OCTAL BUS DRIVER
UC11, 16	2	74S37	IC	QUAD 2-INPUT NAND BUFFERS
UC12	1	30MHZ OSC	OSCILLATOR	30 MHZ OSCILLATOR
UC13, UG9, 15-17	5	74S161	IC	4-BIT COUNTER



Reference No's	Total	Part Name	Part Type	Description
UC14, UG8, 12	3	74S112	IC	DUAL J-K FLIP-FLOP
UC15	1	74S195	IC	4-BIT SHIFT REGISTER
UC17-18, UG6, 20-22	6	74LS161	IC	4-BIT COUNTER
UD1, UE1	2	UPD7220	IC	GRAPHIC DISPLAY CONTROLLER
UD2-3, UE2-3	4	74LS373	IC	OCTAL TRI-STATE LATCH
UD4, UE6	2	74LS02	IC	QUAD 2-INPUT NOR GATE
UD5	1	74S139	IC	DUAL 2-10-4 LINE DECODER
UD6-7, UE4-5	4	74LS74A	IC	DUAL D FLIP-FLOP
UD18-21, UE17-20	8	Am27S191C	IC	2KX8 BIPOLAR PROM
UD23-26, UE22-24, UG23	8	74LS86	IC	QUAD 2-INPUT EXOR GATE
UE26, UF3-4, 7-9, 11, 14, 17	9	25S08	IC	QUAD REGISTER W/ENABLE
UF10	1	74148	IC	8 BIT PRIORITY ENCODER
UF12-13	2	74S153	IC	DUAL 4-1 DATA MULTIPLEXERS
UF15	1	7433	IC	QUAD 2-INPUT NOR BUFFERS W/OC OUTPUTS
UF16	1	74128	IC	QUAD 50-OHM LINE DRIVER
UG2-5	4	74S189	IC	16X4 TTL RAM
UG7	1	74S32	IC	QUAD OR GATE
UG11	1	74LS112	IC	DUAL J-K FLIP-FLOP
UG13-14	2	74F521	IC	8 BIT COMPARATOR
UG19	1	74LS85	IC	4 BIT COMPARATOR
UG26	1	74LS157	IC	QUAD 2-1 DATA MULTIPLEXER



This file contains the fixes for VC1100A. All changes in this file should be made on Version 'A' of the board.

- 1) Problem: The signals VB\_DS0 and VB\_DS1 need to be reversed everywhere except at UG5-7.

Fix:   
✓ Cut wire from UG5-7 on solder side. CK UG5-7 to UC4-13  
✓ Cut wire from UA7-5 on solder side. CK UA7-5 to UC4-11  
Solder Jumper from UA7-5 to UC4-13.  
Solder Jumper from UA7-7 to UC4-11.

- 2) Problem: The signals DMA\_A00 and DMA\_A00X need to be reversed.

Fix:   
✓ Cut wire on LEFT side of UB15-11 on solder side. CK UB15-11 to UC15-13  
✓ Cut wire from UB15-10 on solder side. CK UB15-10 UC 15-11  
Solder Jumper from UB15-11 to UC15-11.  
Solder Jumper from UB15-10 to UC15-13.

- 3) Problem: No pullups on the RAM decoders address inputs.

Fix:   
Solder Jumper from RPG1-9 to JB6-4.  
Solder Jumper from RPG1-10 to JB6-3.

- 4) Problem: UC22-2 and UC24-1 should be DMA\_GRNTD\_LB instead of DMA\_GRNTD\_VB.

Fix:   
✓ Cut wire on RIGHT side of UC24-1 on solder side. CK UC24-1 to UC31-1  
✓ Cut wire BELOW UC22-2 on solder side. CK UC22-2 to UG9-18  
Solder Jumper from UC29-2 to UB13-3.  
Solder Jumper from UC31-1 to UC22-1.  
Solder Jumper from UC31-13 to UC24-1.

- 5) Problem: Include DMA VERSAbus access rights as bit 3 of the DMA mode register.

Fix:   
Solder Jumper from UB14-14 to JB8-2.

- 6) Problem: Reset push-button switch holes and connections were layed out wrong.

Fix:   
Wire push button switch descretely:

0	0	Mounting Holes
(1)	(2)	(3)
0	0	0
(NC)	(COM)	(NO)

Hole 1 should be connected to the Normally Connected switch contact.  
Hole 2 should be connected to the Common switch contact.  
Hole 3 should be connected to the Normally Open switch contact.

- 7) Problem: Read I/O DTACK and write I/O DTACK were reversed.

Fix:   
✓ Cut wire from UC7-5 on solder side. CK UC7-5 to UC12-11  
✓ Cut wire from UC7-10 on solder side. CK UC7-10 to UC11-9  
Solder Jumper from UC12-11 to UC7-10.  
Solder Jumper from UC11-9 to UC7-5.

- 8) Problem: Transceivers that interface the TMS99144 to the local data bus



Fix:

- ✓ Cut wire from UD4-19 on solder side. — CK UD4-19 to UC4-7
- ✓ Cut wire from UD5-19 on component side. — CK UD5-19 to UC4-9
- Solder Jumper from UD7-6 to UD4-19.
- Solder Jumper from UD7-8 to UD5-17.
- Solder Jumper from UD7-4 to UD7-9.
- Solder Jumper from UA19-8 to UD7-9.
- Solder Jumper from UC15-7 to UD7-5.
- Solder Jumper from UC15-9 to UD7-10.
- Solder Jumper from UG11-10 to UA19-10.
- Solder Jumper from UC1-4 to UA19-9.

9) Problem: RS2 and RS0 reversed on TMS9914A chip.

Fix:

- ✓ Cut wire from UD1-6 on component side. — UD1-6 to UA6-12
- ✓ Cut wire from UD1-8 on component side. — UD1-8 to UG7-27
- Solder Jumper from UD1-6 to UA6-16.
- Solder Jumper from UD1-8 to UA6-12.

10) Problem: REN and IFC tied together on TMS9914A and 75162A.

Fix:

- ✓ Cut wire between UD1-22 and UD1-23 on solder side. CK UD1-22 to UD1-23
- ✓ Cut wire between UD1-23 and UD3-20 on solder side. CK UD1-23 to UD3-20
- ✓ Cut wire between UD3-20 and UD3-19 on solder side. CK UD3-20 to UD3-19
- Solder Jumper from UD1-22 to UD3-20.
- Solder Jumper from UD1-23 to UD3-19.

UD3 IS UPSIDE DOWN

11) Problem: Enable input on 9519A is positive logic and it was tied to ground.

Fix:

- ✓ Cut wire between UG7-14 and UG7-13 on solder side. CK UG7-13 to UG7-14

12) Problem: Interrupt acknowledge's level decoder wired incorrectly to interrupt response's Jumper block.

Fix:

- ✓ Cut wire from UG3-15 on solder side. CK UG3-7 to JB4-7
- Solder Jumper from UG3-7 to JB4-7.

13) Problem: When Multi-Wire reversed the power and ground on the AM2940 chips, they forgot to change the wired around connections to the pins on the chips, thus pins that should have been grounded were tied to VCC.

Fix:

- ✓ Cut wire from UB3-8 on solder side. CK UB3-8 TO UB3-20
- ✓ Cut wire from UB4-8 on solder side. CK UB4-8 TO UB4-20
- ✓ Cut two wires from UB5-8 on solder side. CK UB5-8 TO UB5-20, CK UB5-8 TO UB5-6
- Solder Jumper from UB3-22 to UB3-20.
- Solder Jumper from UB4-22 to UB4-20.
- Solder Jumper from UB5-22 to UB5-20.
- Solder Jumper from UB5-20 to UB5-9.

14) Problem: Multi-wire mis-wired IO\_WRX to the front panel logic.

Fix:

- ✓ Cut wire on BOTH sides of UF4-13 on solder side. CK UF4-13 to UB18-2, CK UF4-13 TO UF4-9
- Solder Jumper from UB16-11 to UF4-9.
- Solder Jumper from UC12-10 to UF4-13.



VCI

Total	Part Name	Distributor	Manufacturer	Part Number	P. O. Number	Quantity	Price	Due Date
1	25LS2519	HAMILTON	AMD	25LS2519	✓			
9	25LS2521	HAMILTON	AMD	25LS2521	✓			
1	5 MHZ OSC	HAMILTON	DALE	XO-33D5				
4	74LS00	HAMILTON	ANY	74LS00	✓			
7	74LS02	HAMILTON	ANY	74LS02	✓			
6	74LS04	HAMILTON	ANY	74LS04	✓			
2	74LS08	HAMILTON	ANY	74LS08				
3	74LS10	HAMILTON	ANY	74LS10				
2	74LS11✓	HAMILTON	ANY	74LS11				
7	74LS164✓	HAMILTON	ANY	74LS164				
1	74LS175✓	HAMILTON	ANY	74LS175				
12	74LS240✓	HAMILTON	ANY	74LS240				
5	74LS244✓	HAMILTON	ANY	74LS244				
3	74LS245✓	HAMILTON	ANY	74LS245				
1	74LS30✓	HAMILTON	ANY	74LS30				
3	74LS32✓	HAMILTON	ANY	74LS32				
2	74LS74A✓	HAMILTON	ANY	74LS74A				
1	74LS86✓	HAMILTON	ANY	74LS86				
3	74S02✓	HAMILTON	ANY	74S02				
1	74S138✓	HAMILTON	ANY	74S138				
2	74S139✓	HAMILTON	ANY	74S139				
8	74S240✓	HAMILTON	ANY	74S240				
1	74S260✓	HAMILTON	ANY	74S260				
2	74S38✓	HAMILTON	ANY	74S38				
2	74S74✓	HAMILTON	ANY	74S74				
1	75160A✓	RPS ELECTR	T. I.	75160A				
1	75162A✓	RPS ELECTR	T. I.	75162A				



Total	Part Name	Distributor	Manufacturer	Part Number	P. O. Number	Quantity	Price	Due Date
3	AM2940 ✓	HAMILTON	AMD	AM2940				
1	AM9519A-1 ✓	HAMILTON	AMD	AM9519A-1				
62 X5	C .10F 50V CER .25S	HAMILTON	KEMET	C321C104M5R5CA				
4	JE-10							
2	JE-14							
1	JE-18							
2	JE-2							
1	JE-4							
2	PAL16R4 ✓	HAMILTON	NATIONAL	PAL16R4				
2	R 1K OHM 5% 1/8W							
4	R 3.3K OHM 5% 1/8W							
6	R 3.3K OHM SIP-10							
1	SW DIP-2							
1	SW DIP-4							
2	SW DIP-8							
1	SW PB							
8	TMM2016	JACO	TOSHIBA	TMM2016				
1	TMS9914A	RPS ELECTR	T. I.	TMS9914A				



# VCI

## Component List for VCI100

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Reference No's	Total	Part Name	Part Type	Description
JB1-2, 5, 22	4	JB-10	JUMPER BLK	10 PIN JUMPER BLK
JB3-4	2	JB-14	JUMPER BLK	14 PIN JUMPER BLK
JB6	1	JB-4	JUMPER BLK	4 PIN JUMPER BLOCK
JB7-8	2	JB-2	JUMPER BLK	2 PIN JUMPER BLK
JB10	1	JB-18	JUMPER BLK	18 PIN JUMPER BLK
RA1-2, RD1-2	4	R 3.3K OHM 5% 1/8W	RESISTOR	3.3K OHM 5% 1/8W RESISTOR
RC1, RG1	2	R 1K OHM 5% 1/8W	RESISTOR	3.3K OHM 5% 1/8W RESISTOR
RPA1-3, RPB1, RPC1, RPD1	6	R 3.3K OHM SIP-10	RESISTOR	3.3K OHM SIP RESISTOR PACK
SW1, 3	2	SW DIP-8	SWITCH	8 POSITION DIP SWITCH
SW2	1	SW DIP-4	SWITCH	4 POSITION DIP SWITCH
SW4	1	SW DIP-2	SWITCH	2 POSITION DIP SWITCH
SW9	1	SW PB	SWITCH	PUSH-BUTTON SWITCH
UA1-2, 12-17, UG6	9	25LS2521	IC	8 BIT COMPARATOR
UA3-9, UC4, 15-16, UI1-2	12	74LS240	IC	OCTAL BUS DRIVER
UA10-11, UB9-13, UG9	8	74S240	IC	OCTAL BUS DRIVER
UA18, UG12-13	3	74S02	IC	QUAD 2-INPUT NOR GATE
UA19, UB18	2	74LS08	IC	QUAD 2-INPUT AND GATE
UB1-2, 6-8	5	74LS244	IC	OCTAL BUS DRIVER
UL3-5	3	AM2940	IC	DMA ADDRESS GENERATOR
UB14	1	25LS2519	IC	QUAD REGISTER W/TWO 3-STATE OUTPUTS
UB15, UC11, 21, UE12, UFS, UG11	6	74LS04	IC	HEX INVERTER
UB16-17, UC18, 20, 28, 32, UE2	7	74LS02	IC	QUAD 2-INPUT NOR GATE
UC1, UE1	2	74S139	IC	DUAL 2-TO-4 LINE DECODER
UC2, 7, 29, UE3	4	74LS00	IC	QUAD 2-INPUT NAND GATE
UC3, UG2	2	74S38	IC	QUAD 2-INPUT NAND BUFFER W/OC OUTPUT



## Component List for VCI100

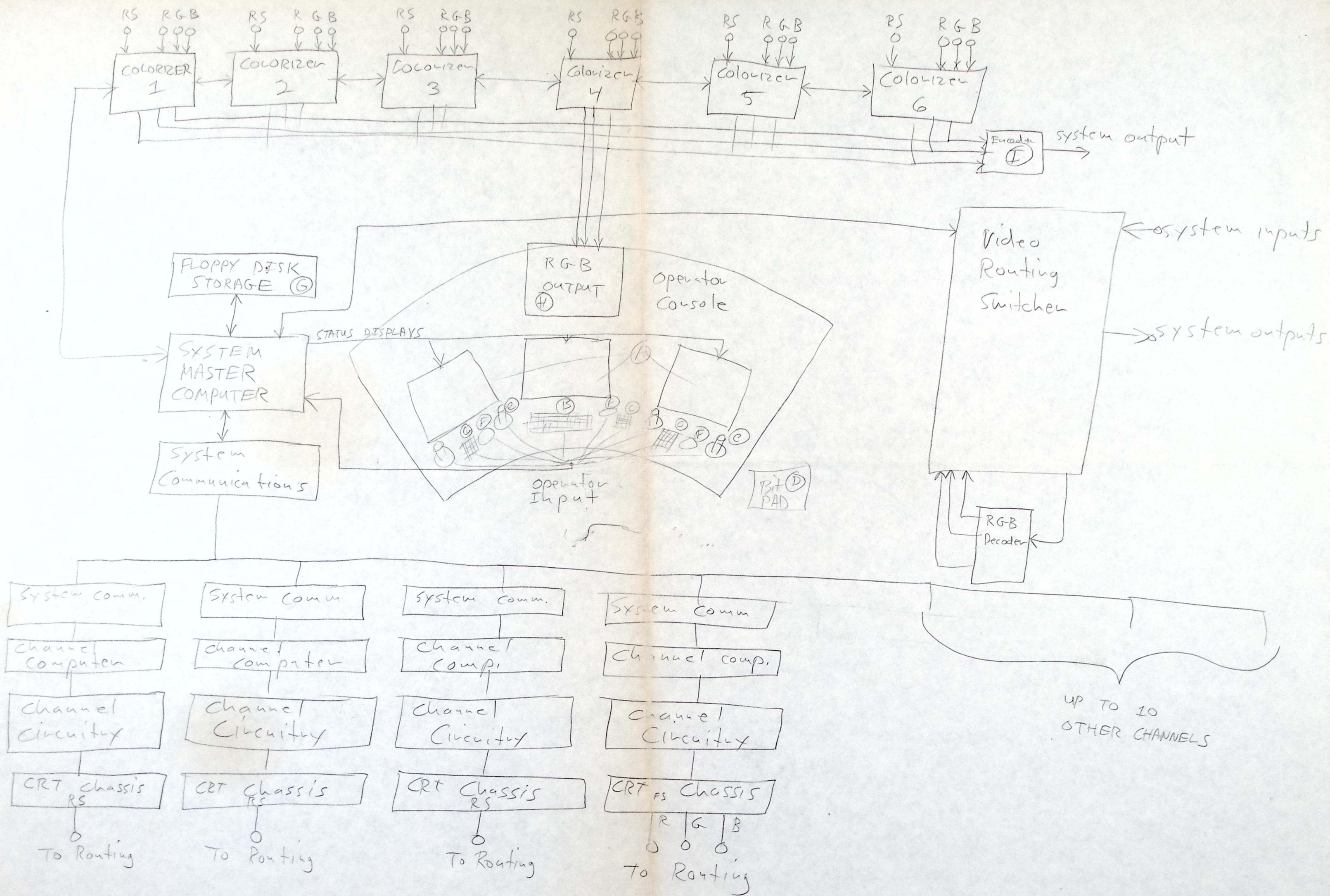
Page 2

Reference No's	Total	Part Name	Part Type	Description
UC5, 30-31	3	74LS10	IC	TRIPLE 3-INPUT NAND GATE
UC6, 17	2	74LS11	IC	TRIPLE 3-INPUT AND GATE
UC9-10, 12-13, 22-24	7	74LS164	IC	8 BIT SERIAL IN/ PARALLEL OUT REGISTER
UC14, UD7, UF4	3	74LS32	IC	QUAD 2-INPUT OR GATE
UC19	1	74S260	IC	DUAL 5-INPUT NOR GATE
UC25, UG10	2	74LS74A	IC	DUAL D FLIP-FLOP
UC26-27	2	74S74	IC	DUAL D FLIP-FLOP
UD1	1	TMS9914A	IC	IEEE-488 CONTROLLER
UD2	1	75160A	IC	IEEE-488 BUS DRIVER
UD3	1	75162A	IC	IEEE-488 BUS DRIVER
UD4-5, UG8	3	74LS245	IC	OCTAL BUS TRANSCEIVER
UD6	1	5 MHZ OSC	OSCILLATOR	5 MHZ OSCILLATOR
UD8	1	74LS86	IC	QUAD 2-INPUT EXOR GATE
UE4-11	8	TMM2016	IC	2KX8 STATIC RAM
UF3	1	74LS175	IC	QUAD REGISTER W/CLEAR
UG1	1	74LS30	IC	8-INPUT NAND GATE
UG3	1	74S138	IC	3-10-8 LINE DECODER
UG4-5	2	PAL16R4	IC	16R4 PAL LOGIC ARRAY
UG7	1	AM9519A-1	IC	INTERRUPT CONTROLLER

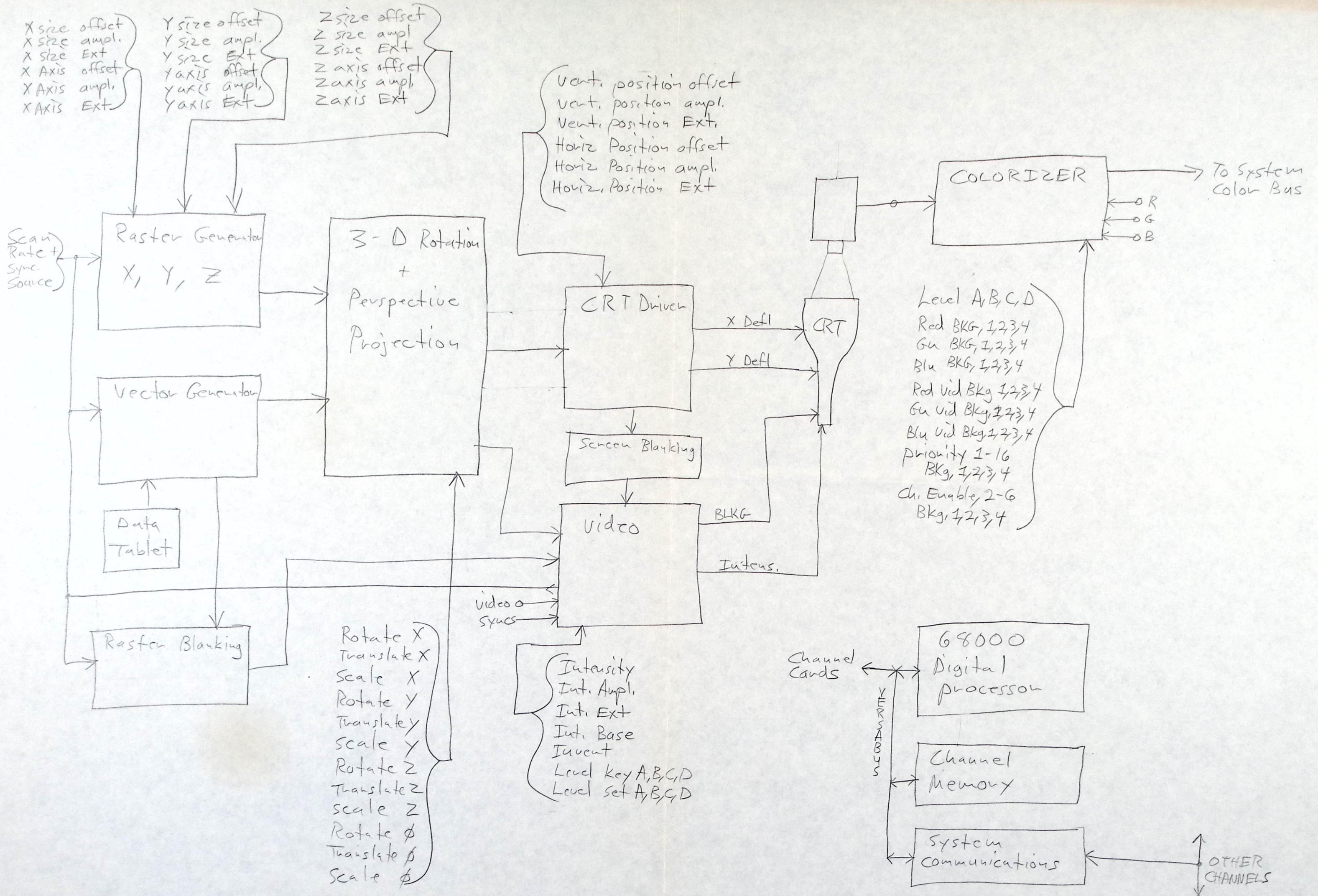


[illegible]

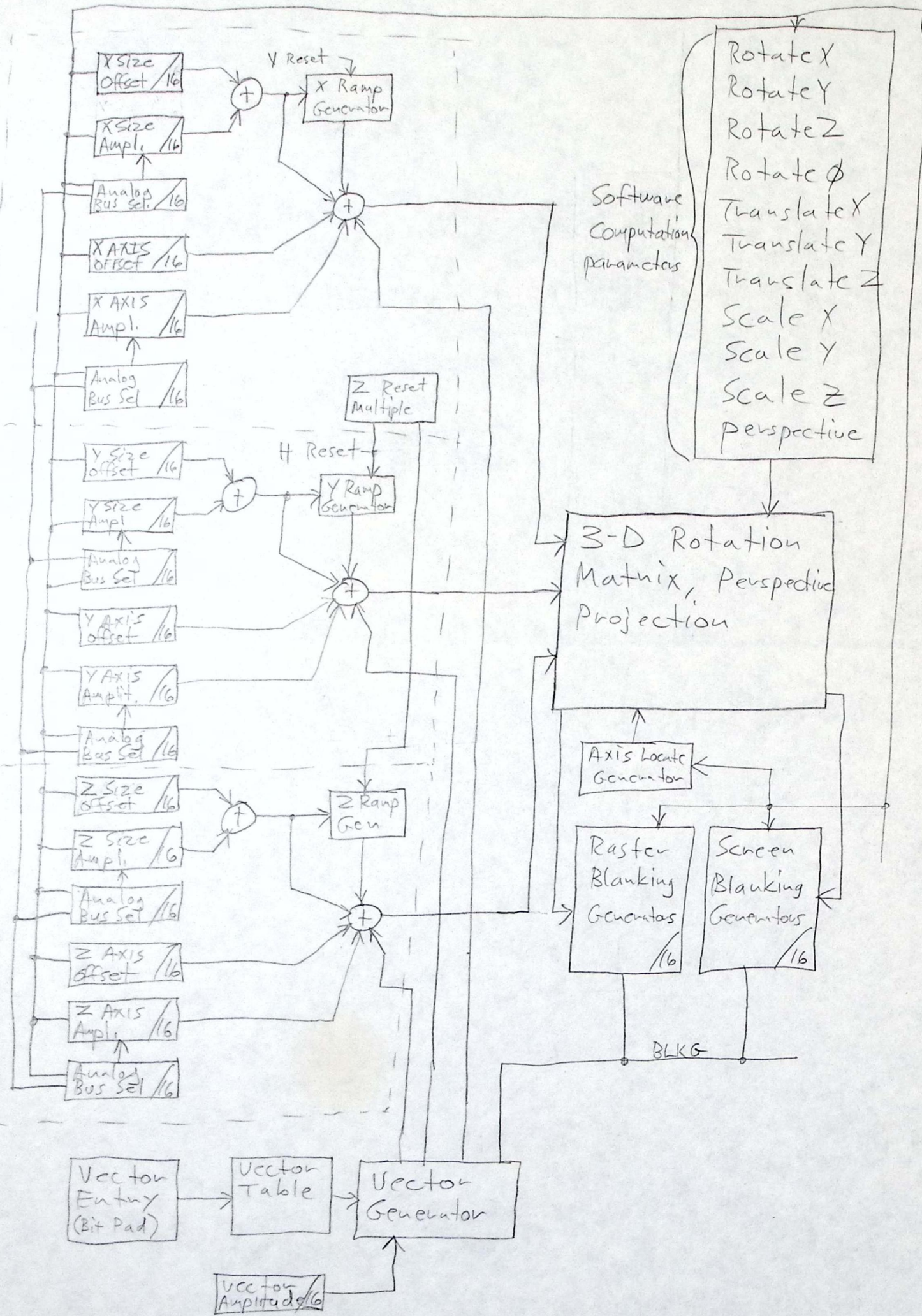




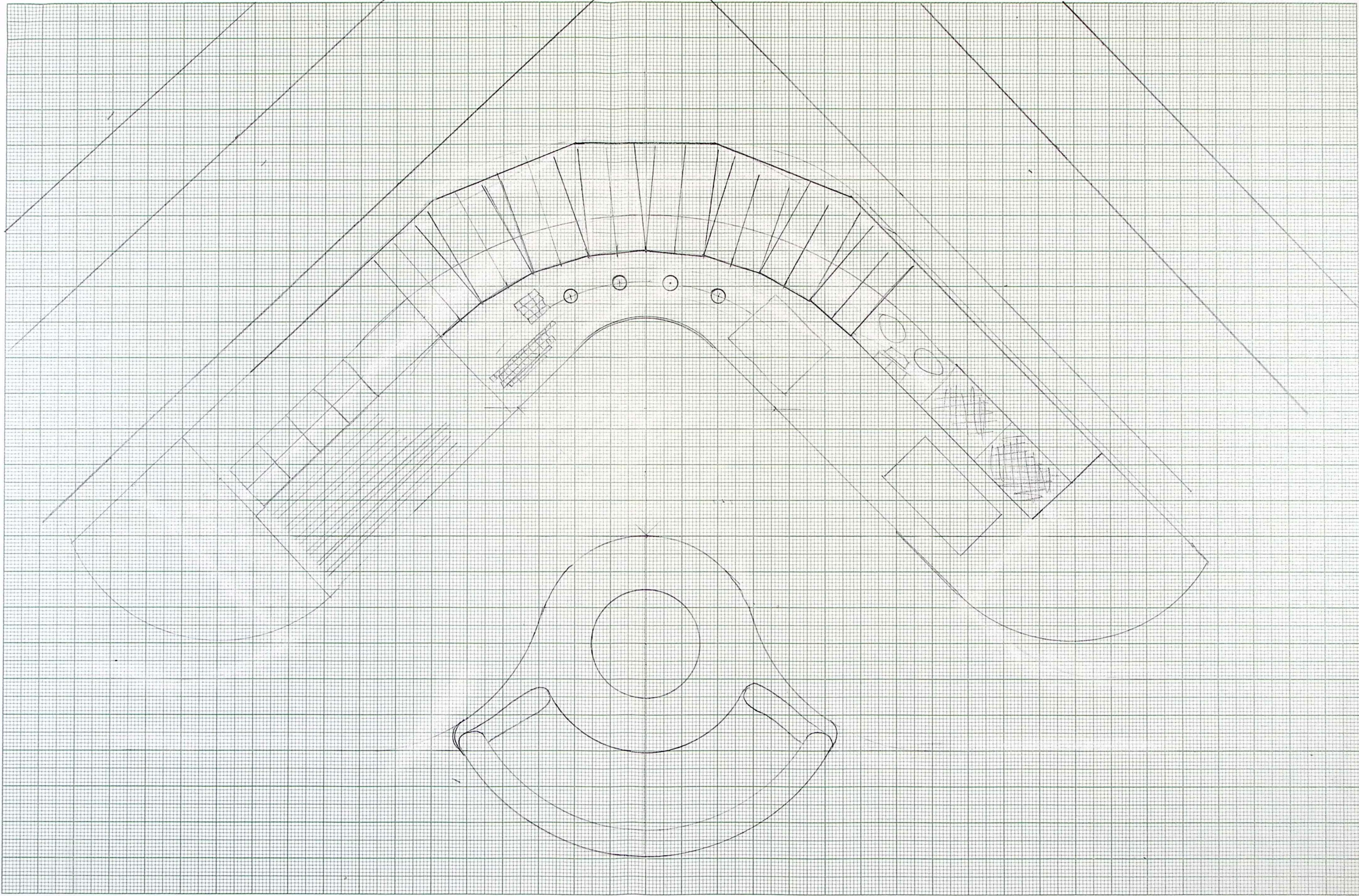




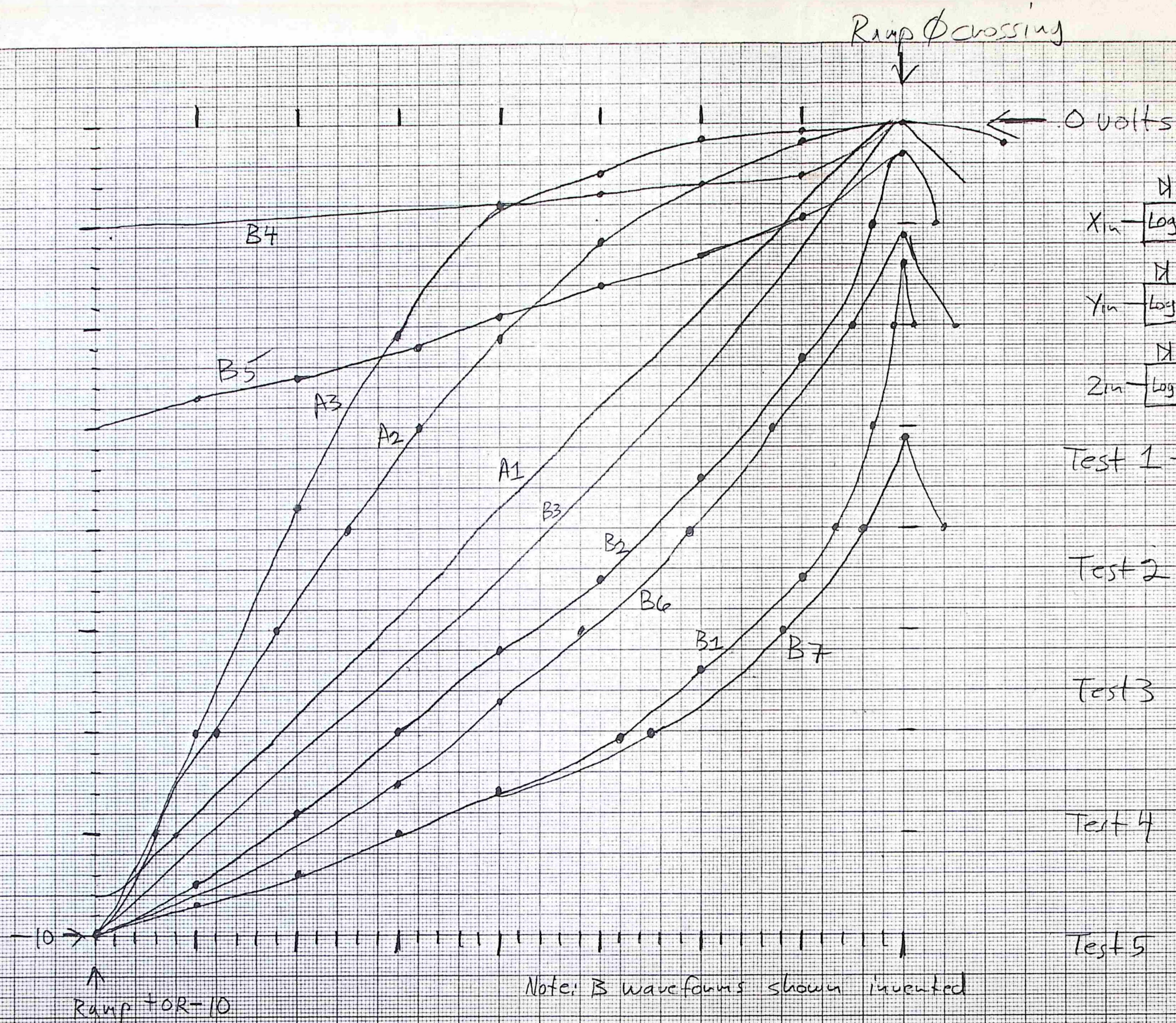




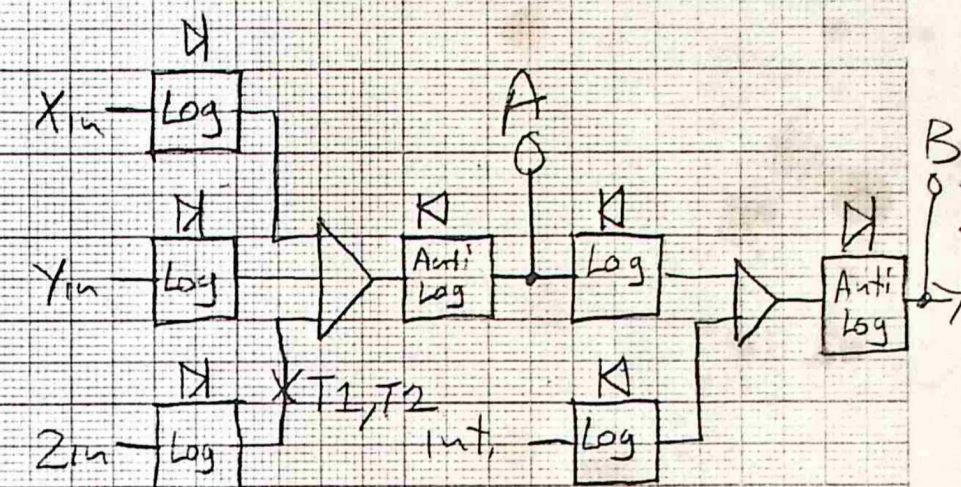








Note: B waveforms shown invented



Test 1 -  $X = \pm 10$  Ramp  
 $Y = +10$  BIAS  
 $Z = N.C.$

Test 6  
 $X = \pm 10$   
 $Y = \pm 10$   
 $Z = +10$  BIAS

Test 2  $X = \pm 10$  Ramp  
 $Y = \pm 10$  Ramp  
 $Z = N.C.$

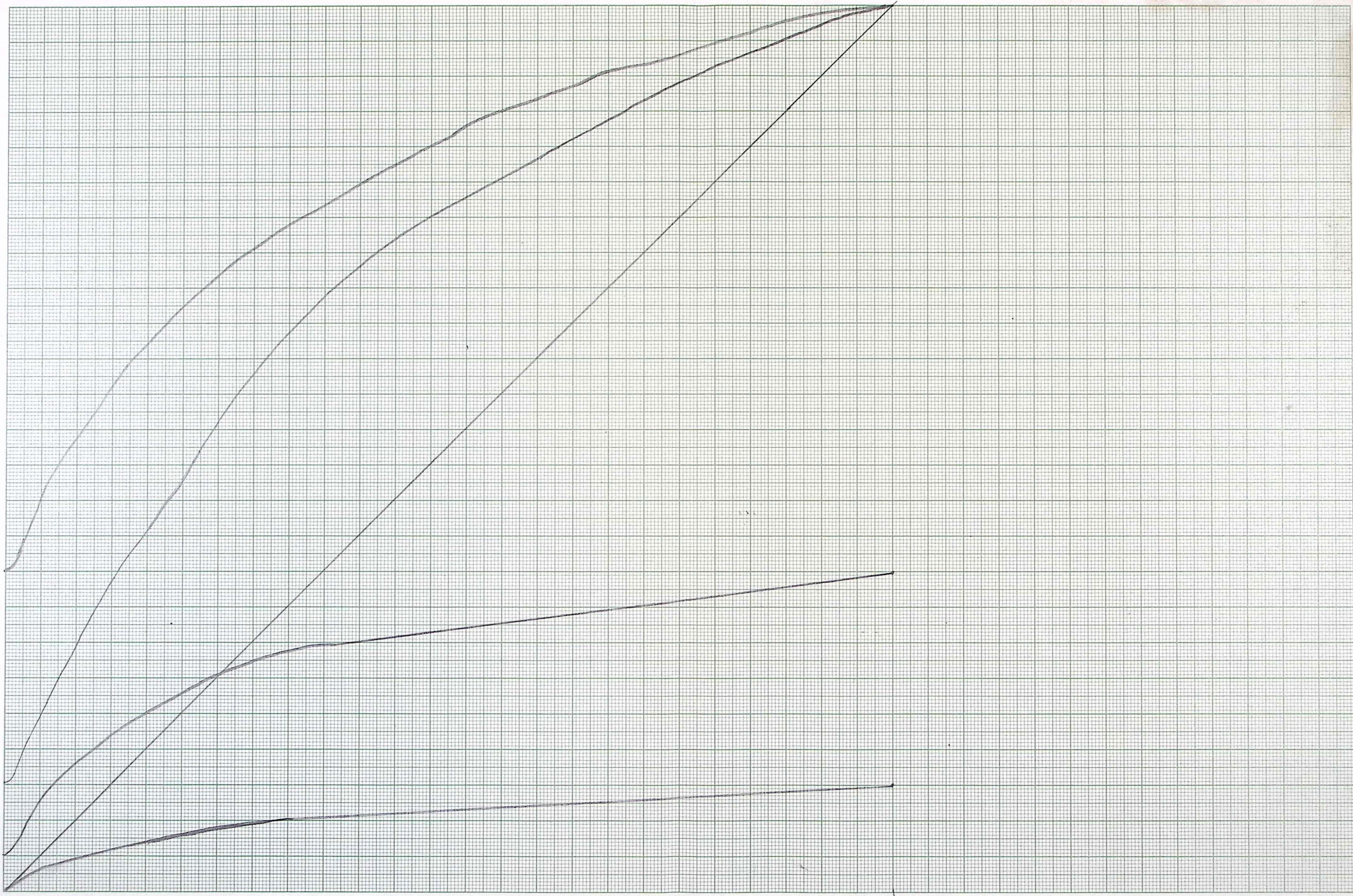
Test 7  
 $X = \pm 10$   
 $Y = +10$   
 $Z = +10$

Test 3  $X = \pm 10V$  Ramp  
 $Y = \pm 10V$  Ramp  
 $Z = \pm 10V$  Ramp

Test 4  $X = \pm 10V$  Ramp  
 $Y = 0V$   
 $Z = N.C.$

Test 5  $X = \pm 10V$  Ramp  
 $Y = \pm 10V$  Ramp  
 $Z = 0V$





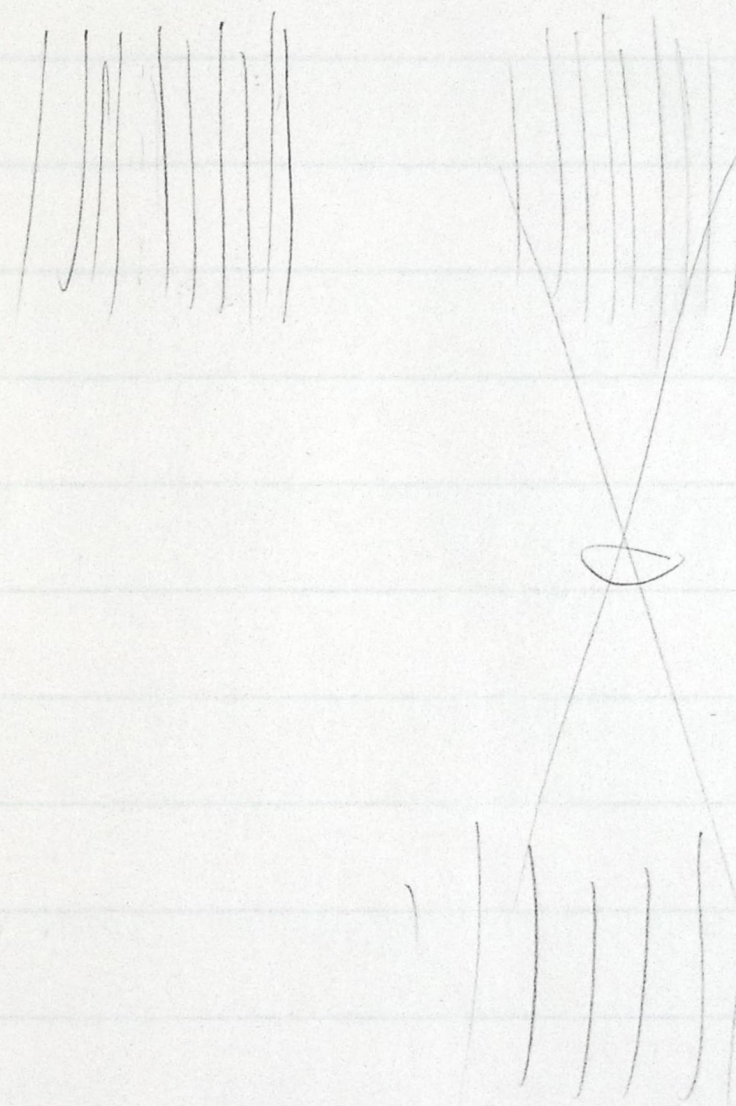


# CONNECTIONS BETWEEN MONOBOARD OUTSIDE WORLD.

## CONNECTOR - A

ALL EVEN NUMBER PINS ARE GROUND.  
CONNECTOR IS 3M PART # 3426-0000  
50 PIN PCB CONNECTOR.

PIN NO.	DESCRIPTION	DESTINATION	COMMENTS
1	GND	E-1	
3	TXD1	E-2	
5	RXD1	E-3	
7	RTS1	E-4	
9	CTS1	E-5	
11	DSR1	E-6	
13	GND	E-7	
15	DCD1	E-8	
17	DTR1	E-20	
19	RXC1	E-17	
21	TXC1	E-15 & E-24	
23	OUTPUT 3	H-7	
25	GATE 3	H-41	
27	CLOCK 3	H-45	
29	GND	F-1	
31	TXD2	F-2	
33	RXD2	F-3	
35	RTS2	F-4	
37	CTS2	F-5	
39	DSR2	F-6	
41	GND	F-7	
43	DCD2	F-8	
45	DTR2	F-20	
47	RXC2	F-17	
49	TXC2	F-15 & F-24	



## CONNECTOR - B

ALL EVEN NUMBER PINS ARE GROUND.  
CONNECTOR IS 3M PART # 3426-0000



## 50 PIN PCB CONNECTOR.

PIN NO.	DESCRIPTION	DESTINATION	COMMENTS
1	P1CB2	G-1	
3	GND	N/C	
5	P1CB1	G-5	
7	GND	N/C	
9	P1PB7	G-9	
11	P1PB6	G-11	
13	P1PB5	G-13	
15	P1PB4	G-15	
17	P1PB3	G-17	
19	P1PB2	G-19	
21	P1PB1	G-21	
23	P1PB0	G-23	
25	P1PA7	G-25	
27	P1PA6	G-27	
29	P1PA5	G-29	
31	P1PA4	G-31	
33	P1PA3	G-33	
35	P1PA2	G-35	
37	P1PA1	G-37	
39	P1PA0	G-39	
41	GND	N/C	
43	P1CA2	G-43	
45	GND	N/C	
47	P1CA1	G-47	
49	GND	N/C	

## CONNECTOR - C

ALL EVEN NUMBER PINS ARE GROUND.  
CONNECTOR IS 3M PART # 3426-0000  
50 PIN PCB CONNECTOR.

PIN NO.	DESCRIPTION	DESTINATION	COMMENTS
---------	-------------	-------------	----------



1	GND	N/C
3	SD-	N/C
5	SD+	N/C
7	ST-	N/C
9	ST+	N/C
11	RD-	N/C
13	RD+	N/C
15	RS-	N/C
17	RS+	N/C
19	RT-	N/C
21	RT+	N/C
23	CS-	N/C
25	CS+	N/C
27	DM-	N/C
29	DM+	N/C
31	TR-	N/C
33	TR+	N/C
35	RR-	N/C
37	RR+	N/C
39	OUTPUT 2	G-45
41	GATE 2	G-49
43	CLOCK 2	H-3
45	OUTPUT 1	G-3
47	GATE 1	G-7
49	CLOCK 1	G-41

# CONNECTOR - D

ALL EVEN NUMBER PINS ARE GROUND.  
CONNECTOR IS 3M # 3426-0000  
50 PIN PCB CONNECTOR.

PIN NO.	DESCRIPTION	DESTINATION	COMMENTS
1	P2CB2	H-1	
3	GND	N/C	
5	P2CB1	H-5	



7	GND	N/C
9	P2PB7	H-9
11	P2PB6	H-11
13	P2PB5	H-13
15	P2PB4	H-15
17	P2PB3	H-17
19	P2PB2	H-19
21	P2PB1	H-21
23	P2PB0	H-23
25	P2PA7	H-25
27	P2PA6	H-27
29	P2PA5	H-29
31	P2PA4	H-31
33	P2PA3	H-33
35	P2PA2	H-35
37	P2PA1	H-37
39	P2PA0	H-39
41	GND	N/C
43	P2CA2	H-43
45	GND	N/C
47	P2CA1	H-47
49	GND	N/C

# CONNECTOR - E

CONNECTOR IS 3M PART # 3426-0000  
26 PIN PCB CONNECTOR.

PIN NO.	DESCRIPTION	DESTINATION	COMMENTS
1	GND	A-1	
2	TXD1	A-3	
3	RXD1	A-5	
4	RTS1	A-7	
5	CTS1	A-9	
6	DSR1	A-11	
7	GND	A-13	



8	DCD1	A-15
9	NO CONNECTION	
10	NO CONNECTION	
11	NO CONNECTION	
12	NO CONNECTION	
13	NO CONNECTION	
14	NO CONNECTION	
15	TXC1	A-21
16	NO CONNECTION	
17	RXC1	A-19
18	NO CONNECTION	
19	NO CONNECTION	
20	DTR1	A-17
21	NO CONNECTION	
22	NO CONNECTION	
23	NO CONNECTION	
24	TXC1	A-21
25	NO CONNECTION	
26	NO CONNECTION	

# CONNECTOR - F

CONNECTOR IS 3M PART # 3434-0000  
26 PIN PCB CONNECTOR.

PIN NO.	DESCRIPTION	DESTINATION	COMMENTS
1	GND	A-29	
2	TXD2	A-31	
3	RXD2	A-33	
4	RTS2	A-35	
5	CTS2	A-37	
6	DSR2	A-39	
7	GND	A-41	
8	DCD2	A-43	
9	NO CONNECTION		
10	NO CONNECTION		



11	NO CONNECTION	
12	NO CONNECTION	
13	NO CONNECTION	
14	NO CONNECTION	
15	TXC2	A-49
16	NO CONNECTION	
17	RXC2	A-47
18	NO CONNECTION	
19	NO CONNECTION	
20	DTR2	A-45
21	NO CONNECTION	
22	NO CONNECTION	
23	NO CONNECTION	
24	TXC2	A-49
25	NO CONNECTION	
26	NO CONNECTION	

# CONNECTOR - G

ALL EVEN PIN NUMBERS ARE GROUND.  
CONNECTOR IS 3M PART # 3426-0000  
50 PIN PCB CONNECTOR.

PIN NO.	DESCRIPTION	DESTINATION	COMMENTS
1	P1CB2	B-1	INT. INPUT
3	OUTPUT 1	C-45	CLOCK 1 OUTPUT
5	P1CB1	B-5	FIELD IDENT INTERRUPT
7	GATE 1	C-47	CLOCK 1 INPUT
9	P1PB7	B-9	ADDR 15
11	P1PB6	B-11	ADDR 14
13	P1PB5	B-13	ADDR 13
15	P1PB4	B-15	ADDR 12
17	P1PB3	B-17	ADDR 11
19	P1PB2	B-19	ADDR 10
21	P1PB1	B-21	ADDR 09
23	P1PB0	B-23	ADDR 08



25	F1PA7	B-25	ADDR 07
27	F1PA6	B-27	ADDR 06
29	F1PA5	B-29	ADDR 05
31	F1PA4	B-31	ADDR 04
33	F1PA3	B-33	ADDR 03
35	F1PA2	B-35	ADDR 02
37	F1PA1	B-37	ADDR 01
39	F1PA0	B-39	ADDR 00
41	CLOCK 1	C-49	CLOCK 1 INPUT
43	F1CA2	B-43	INT. INPUT
45	OUTPUT 2	C-39	CLOCK 2 OUTPUT
47	F1CA1	B-47	END OF FIELD INTERRUPT
49	GATE 2	C-41	CLOCK 2 INPUT

# CONNECTOR - H

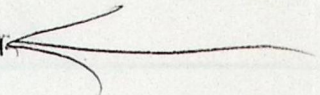
ALL EVEN PIN NUMBERS ARE GROUND.  
CONNECTOR IS 3M PART # 3426-0000  
50 PIN PCB CONNECTOR.

PIN NO.	DESCRIPTION	DESTINATION	COMMENTS
1	P2CB2	D-1	DATA STROBE
3	CLOCK 2	C-43	CLOCK 2 INPUT
5	P2CB1	D-5	INT. INPUT
7	OUTPUT 3	A-23	CLOCK 3 OUTPUT
9	P2PB7	D-9	DATA 15
11	P2PB6	D-11	DATA 14
13	P2PB5	D-13	DATA 13
15	P2PB4	D-15	DATA 12
17	P2PB3	D-17	DATA 11
19	P2PB2	D-19	DATA 10
21	P2PB1	D-21	DATA 09
23	P2PB0	D-23	DATA 08
25	P2PA7	D-25	DATA 07
27	P2PA6	D-27	DATA 06
29	P2PA5	D-29	DATA 05

← FB



31	P2PA4	D-31	DATA 04
33	P2PA3	D-33	DATA 03
35	P2PA2	D-35	DATA 02
37	P2PA1	D-37	DATA 01
39	P2PA0	D-39	DATA 00
41	GATE 3	A-25	CLOCK 3 INPUT
43	P2CA2	D-43	INT. INPUT
45	CLOCK 3	A-27	CLOCK 3 INPUT
47	P2CA1	D-47	INT. INPUT
49	GND		





SLAVE HARDWARE DESCRIPTION  
JANUARY 7, 1982



SLAVE HARDWARE DESCRIPTION  
TABLE OF CONTENTS

JANUARY 7, 1982

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TIMING & BLANKING CARD.....	0009
INTERFACE CARD.....	0010



RESCAN CHANNEL:    ALL PARAMETERS CAN EFFECT AS MANY AS SIXTEEN RASTER  
SEGMENTS OF VARIABLE LENGTH AT A TIME.

FLYING SPOT CHANNEL: ALL PARAMETERS EFFECT THE ENTIRE RASTER. NO SEGMENTING  
IS AVAILABLE.

	OFFSET	AMPLITUDE	CONNECTION
X AXIS	0 - 4095	0 - 4095	0 - 31
Y AXIS	0 - 4095	0 - 4095	0 - 31
Z AXIS	0 - 4095	0 - 4095	0 - 31
X SIZE	0 - 4095	0 - 4095	0 - 31
Y SIZE	0 - 4095	0 - 4095	0 - 31
Z SIZE	0 - 4095	0 - 4095	0 - 31



RESCAN CHANNEL: ALL PARAMETERS CAN EFFECT AS MANY AS SIXTEEN RASTER  
SEGMENTS OF VARIABLE LENGTH AT A TIME.

FLYING SPOT CHANNEL: ALL PARAMETERS EFFECT THE ENTIRE RASTER. NO SEGMENTING  
IS AVAILABLE.

	OFFSET	AMPLITUDE	CONNECTION
HORIZONTAL POSITION	0 - 4095	0 - 4095	0 - 31
VERTICAL POSITION	0 - 4095	0 - 4095	0 - 31
INTENSITY	0 - 4095	0 - 4095	0 - 31
BLANKING FIXED TO SCREEN			
+ X EDGE	0 - 4095		
- X EDGE	0 - 4095		
+ Y EDGE	0 - 4095		
- Y EDGE	0 - 4095		
+ Z EDGE	0 - 4095		
- Z EDGE	0 - 4095		



FOR BOTH THE RESCAN AND FLYING SPOT CHANNELS SCAN RATES ARE SELECTABLE.

THERE ARE 3 FOUR POSITION SWITCHES:

HI-RES HORIZONTAL

- GENERATOR HI-RES
- PROGRAMMABLE
- GRAPHICS
- SYNC STRIPED HORIZONTAL

LO-RES HORIZONTAL

- GENERATOR LO-RES
- PROGRAMMABLE
- SPARE
- SYNC STRIPED HORIZONTAL

VERTICAL

- GENERATOR
- SPARE
- SPARE
- SYNC STRIPED VERTICAL

RESCAN CHANNEL FUNCTIONS:

GAMMA	0 - 255
LEVEL 1 ENCODE	0 - 255
LEVEL 2 ENCODE	0 - 255
LEVEL 3 ENCODE	0 - 255
LEVEL 4 ENCODE	0 - 255
GRAY 1 INTENSITY	0 - 255
GRAY 2 INTENSITY	0 - 255
GRAY 3 INTENSITY	0 - 255
GRAY 4 INTENSITY	0 - 255
GRAY 5 INTENSITY	0 - 255

CONTROL REGISTER

BIT

- 0 - NORMAL / INVERT

FLYING SPOT CHANNEL FUNCTIONS:

GAMMA 1	0 - 255
GAMMA 2	0 - 255
GAMMA 3	0 - 255

CONTROL REGISTER

BIT

- 0 - NORMAL / INVERT 1
- 1 - NORMAL / INVERT 2
- 2 - NORMAL / INVERT 3



THERE ARE FOUR SETS OF RAMS TO HOLD THE X, Y, Z, AND INTENSITY FOR EACH VECTOR END POINT. EACH RAM SET WILL HOLD 512 VECTOR POINTS.

THE RAM SETS FOR X, Y, AND Z:

START POINT 2	START POINT 1	END POINT 2	END POINT 1
START POINT 4	START POINT 3	END POINT 4	END POINT 3
START POINT 6	START POINT 5	END POINT 6	END POINT 5
.	.	.	.
.	.	.	.
START POINT N	START POINT N-1	END POINT N	END POINT N-1

THE RAM SET FOR INTENSITY:

POINT 2	POINT 1
POINT 4	POINT 3
POINT 6	POINT 5
.	.
.	.
POINT N	POINT N-1

VECTORS OFF <—> ON

0 - 4095

CONTROL REGISTER

BIT

5 - BLANKING  
6 - INTENSITY ZERO BLANKING  
7 - STOP COUNT BLANKING

ENABLE/DISABLE  
ENABLE/DISABLE  
ENABLE/DISABLE



RESCAN CHANNEL: ALL PARAMETERS CAN EFFECT AS MANY AS SIXTEEN RASTER  
SEGMENTS OF VARIABLE LENGTH AT A TIME.

FLYING SPOT CHANNEL: ALL PARAMETERS EFFECT THE ENTIRE RASTER. NO SEGMENTING  
IS AVAILABLE.

	OFFSET
A LINEAR TRANSFORMATION	0 - 4095
B LINEAR TRANSFORMATION	0 - 4095
C LINEAR TRANSFORMATION	0 - 4095
D LINEAR TRANSFORMATION	0 - 4095
E LINEAR TRANSFORMATION	0 - 4095
F LINEAR TRANSFORMATION	0 - 4095
G LINEAR TRANSFORMATION	0 - 4095
H LINEAR TRANSFORMATION	0 - 4095
I LINEAR TRANSFORMATION	0 - 4095
X PERSPECTIVE	0 - 4095
Y PERSPECTIVE	0 - 4095
Z PERSPECTIVE	0 - 4095
X TRANSLATION	0 - 4095
Y TRANSLATION	0 - 4095
Z TRANSLATION	0 - 4095
OVERALL SCALING	0 - 4095



RESCAN CHANNEL: ALL PARAMETERS EFFECT THE ENTIRE RASTER.

FLYING SPOT CHANNEL: ALL PARAMETERS EFFECT THE ENTIRE RASTER.

	OFFSET
RED BACKGROUND OFFSET	255 - 0
RED LEVEL 1 OFFSET	255 - 0
RED LEVEL 2 OFFSET	255 - 0
RED LEVEL 3 OFFSET	255 - 0
RED LEVEL 4 OFFSET	255 - 0
GREEN BACKGROUND OFFSET	255 - 0
GREEN LEVEL 1 OFFSET	255 - 0
GREEN LEVEL 2 OFFSET	255 - 0
GREEN LEVEL 3 OFFSET	255 - 0
GREEN LEVEL 4 OFFSET	255 - 0
BLUE BACKGROUND OFFSET	255 - 0
BLUE LEVEL 1 OFFSET	255 - 0
BLUE LEVEL 2 OFFSET	255 - 0
BLUE LEVEL 3 OFFSET	255 - 0
BLUE LEVEL 4 OFFSET	255 - 0
RED BACKGROUND VIDEO AMPLITUDE	0 - 255
RED LEVEL 1 VIDEO AMPLITUDE	0 - 255
RED LEVEL 2 VIDEO AMPLITUDE	0 - 255
RED LEVEL 3 VIDEO AMPLITUDE	0 - 255
RED LEVEL 4 VIDEO AMPLITUDE	0 - 255
GREEN BACKGROUND VIDEO AMPLITUDE	0 - 255
GREEN LEVEL 1 VIDEO AMPLITUDE	0 - 255
GREEN LEVEL 2 VIDEO AMPLITUDE	0 - 255
GREEN LEVEL 3 VIDEO AMPLITUDE	0 - 255
GREEN LEVEL 4 VIDEO AMPLITUDE	0 - 255
BLUE BACKGROUND VIDEO AMPLITUDE	0 - 255
BLUE LEVEL 1 VIDEO AMPLITUDE	0 - 255
BLUE LEVEL 2 VIDEO AMPLITUDE	0 - 255
BLUE LEVEL 3 VIDEO AMPLITUDE	0 - 255
BLUE LEVEL 4 VIDEO AMPLITUDE	0 - 255
LEVEL 1 ENCODE	0 - 255
LEVEL 2 ENCODE	0 - 255
LEVEL 3 ENCODE	0 - 255
LEVEL 4 ENCODE	0 - 255
BACKGROUND PRIORITY	255 - 0
LEVEL 1 PRIORITY	255 - 0
LEVEL 2 PRIORITY	255 - 0
LEVEL 3 PRIORITY	255 - 0
LEVEL 4 PRIORITY	255 - 0



CONTROL REGISTERS

BIT

- 0 - ENABLE VIDEO IN BACKGROUND
- 1 - ENABLE VIDEO IN LEVEL 1
- 2 - ENABLE VIDEO IN LEVEL 2
- 3 - ENABLE VIDEO IN LEVEL 3
- 4 - ENABLE VIDEO IN LEVEL 4

	REG1	REG2	REG3	REG4	REG5
COLORIZER 1 -	2	3	4	5	6
COLORIZER 2 -	1	3	4	5	6
COLORIZER 3 -	1	2	4	5	6
COLORIZER 4 -	1	2	3	5	6
COLORIZER 5 -	1	2	3	4	6
COLORIZER 6 -	1	2	3	4	5



THERE ARE SIXTEEN OSCILLATORS, EACH HAVING THE FOLLOWING PARAMETERS:

	OFFSET
OFFSET	0 - 4095
GAIN	0 - 4095
FREQUENCY	0 - 4095
PHASE LOCK POINT	0 - 4095
OFFSET MODULATION SOURCE	0 - 31
GAIN MODULATION SOURCE	0 - 31
PHASE LOCK SELECT	0 - 31

CONTROL REGISTERS

BITS	
0 - 3	PHASE LOCK MULTIPLE 0 - 15
4 & 5	WAVEFORM SELECT 0 - 3
6	OFFSET FULL WAVE RECTIFIER ON/OFF
7	GAIN FULL WAVE RECTIFIER ON/OFF



RESCAN CHANNEL: THE BLANKING PARAMETERS CAN EFFECT AS MANY AS SIXTEEN  
RASTER SEGMENTS OF VARIABLE LENGTH AT A TIME.

FLYING SPOT CHANNEL: THE BLANKING PARAMETERS EFFECT THE ENTIRE RASTER.  
NO SEGMENTING IS AVAILABLE.

BLANKING FIXED TO RASTER	OFFSET
+ X EDGE	0 - 4095
- X EDGE	0 - 4095
+ Y EDGE	0 - 4095
- Y EDGE	0 - 4095
+ Z EDGE	0 - 4095
- Z EDGE	0 - 4095

THE TIMING CARD PROVIDES TIMING SIGNALS FOR THE ENTIRE SYSTEM.  
THERE ARE FIFTEEN SEGMENT CHANGE REGISTERS WHICH CONTAIN THE  
NUMBER OF THE LAST LINE OF ALL OF THE SEGMENTS EXCEPT SEGMENT  
SIXTEEN WHICH BY CONVENTION IS THE LAST LINE OF THE VIDEO.  
THERE IS ONE SCAN BAR ADJUST REGISTER, ONE TEST & TRIGGER  
REGISTER AND ONE CONTROL REGISTER.

	OFFSET
SEGMENT CHANGE	0 - 1023
SCAN BAR ADJUST	0 - 1023
Z RAMP RATE	0 - 4095

#### TEST & TRIGGER REGISTER

BITS	
0 - 4	TEST LINE SELECT
5 - 7	TRIGGER SELECT

#### CONTROL REGISTER

BITS		
0	HIGH RESOLUTION	ON/OFF
1	SECTION VERTICAL RESET	ENABLE/DISABLE
2	VERTICAL AXIS LOCATE	ENABLE/DISABLE
3	BLANK OFF CRT	ENABLE/DISABLE
4	Z RESET ENABLE	ENABLE/DISABLE
5	STANDARD BLANKING	ENABLE/DISABLE
6	RASTER RELATIVE BLANKING	ENABLE/DISABLE
7	SCREEN RELATIVE BLANKING	ENABLE/DISABLE



SLAVE HARDWARE DESCRIPTION  
INTERFACE CARD

JANUARY 7, 1982

0010

8 INTERRUPT VECTORS  
BASE REGISTER  
DMA CONTROL REGISTER  
DMA REGISTERS  
488 CHIP  
8K X 16 RAM



VTE-100 POWER & GROUND

PLUS 5 VOLT CONNECTIONS:

J1 - 1, 2, 129, 130, 131, 132.

J2 - 7, 8, 9, 10.

GROUND CONNECTIONS:

J1 - 3, 4, 23, 24, 27, 28, 31, 32, 61, 62, 67, 68, 71, 72, 119  
120, 123, 124, 135, 136, 137, 138, 139, 140.

J2 - 1, 2, 3, 4, 5, 6, 13, 14

PLUS 15 VOLT CONNECTIONS:

J2 - ~~67, 68~~ 69, 70

Minus 15 VOLT CONNECTIONS:

J2 - 67, 68

(Colonizer



VTE-100 POWER & GROUND

PLUS 5 VOLT CONNECTIONS:

J1 - 1, 2, 129, 130, 131, 132.

J2 - 7, 8, 9, 10.

GROUND CONNECTIONS:

J1 - 3, 4, 23, 24, 27, 28, 31, 32, 61, 62, 67, 68, 71, 72, 119

120, 123, 124, 135, 136, 137, 138, 139, 140.

J2 - 1, 2, 3, 4, 5, 6.



